

Model: Mission Hills/Sawgrass

PCB Ver: A00

PCB Number: 10097-1

SCH Ver: 06

PCBA:

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50	CPU VRD 12-1 & CPU AXG	
51	CPU_VRD 12-2	

PCB BOARD SIZE
4 Layers
244mmX 218mm

BOM Configuration
Unmount: (R)
Unmount after MP (X)

SB BUILD

Sugar Bay :

LGA1155 : Sandy Brighe

Chipset : Cougar Point H61

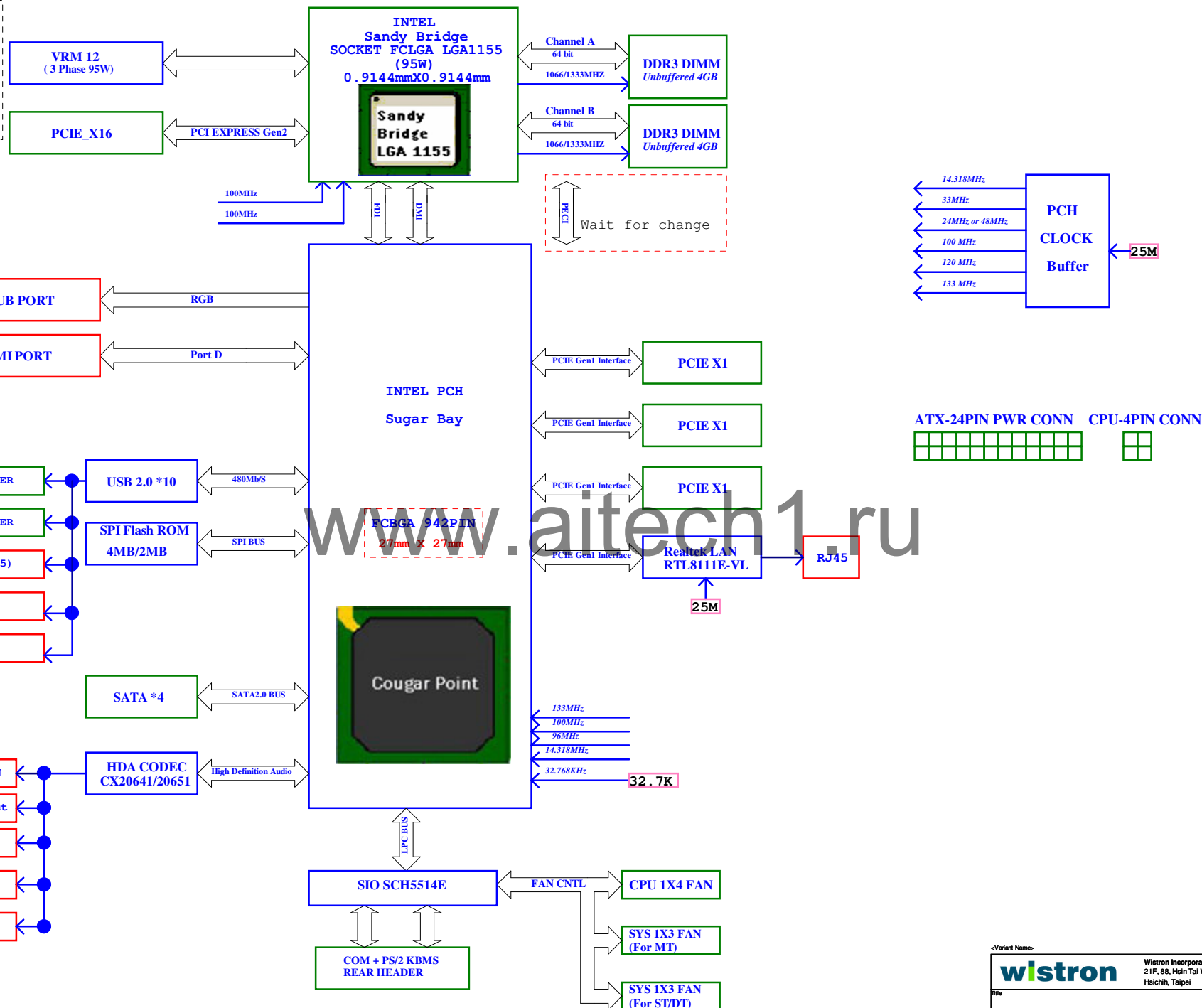
LAN : Gb LAN RTL8151ED

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Title			
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PCB BOARD SIZE
244mmX 218mm
4 Layer

Internal Slot/Header
Front/Rear IO
Chipset



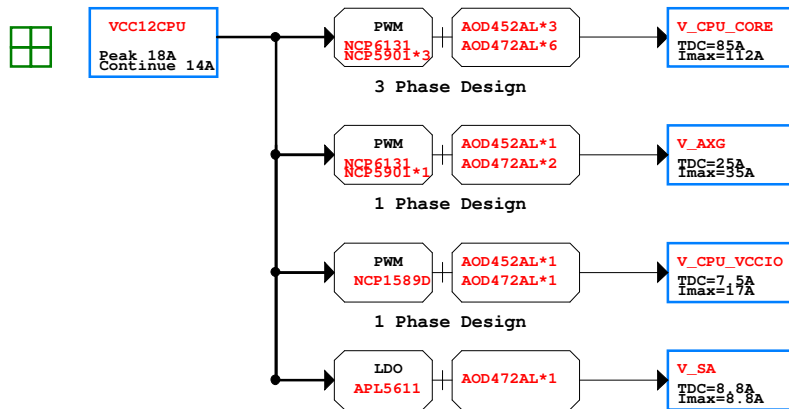
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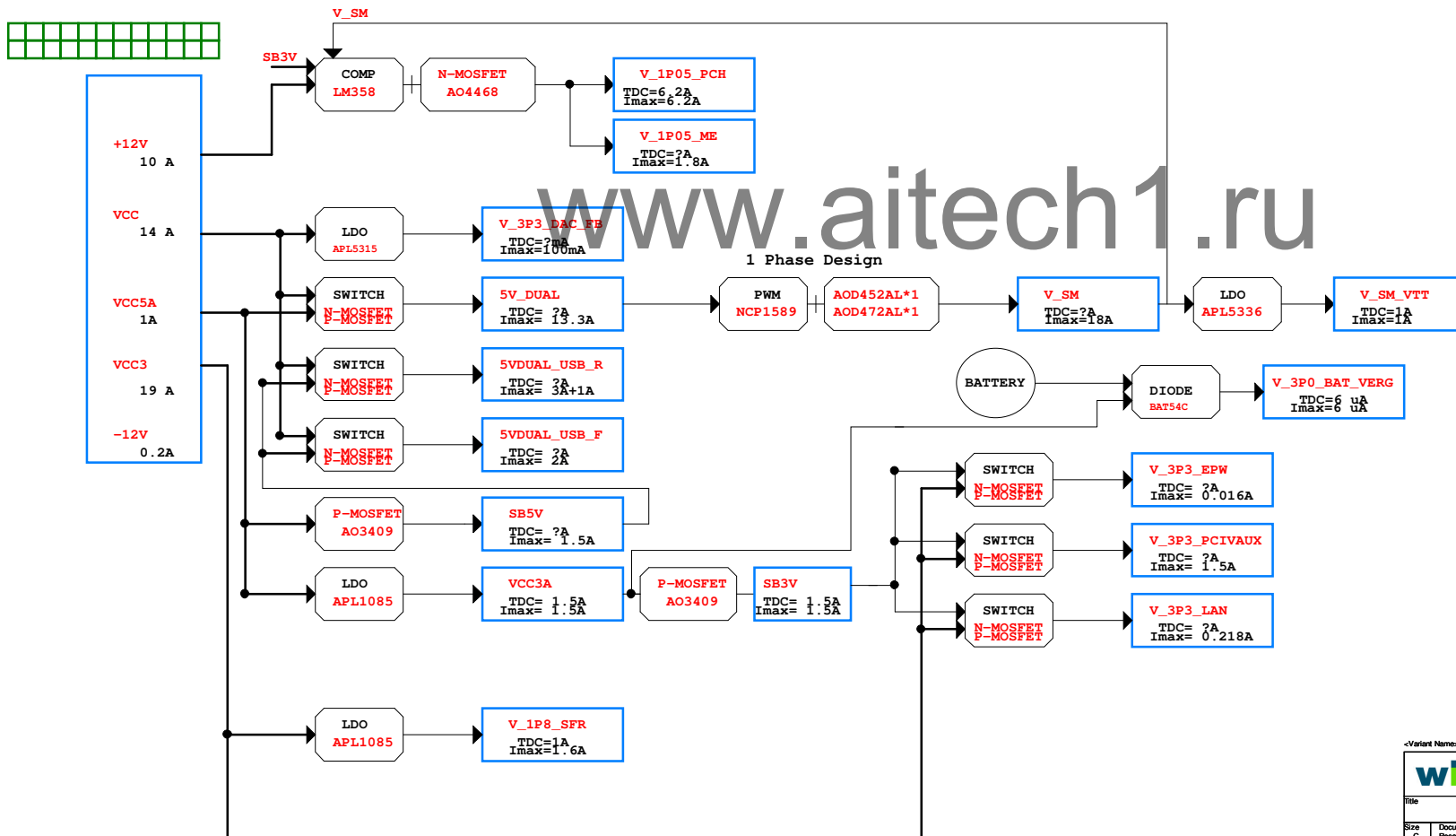
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CPU 2X2 POWER CONN



ATX 2X12 POWER CONN



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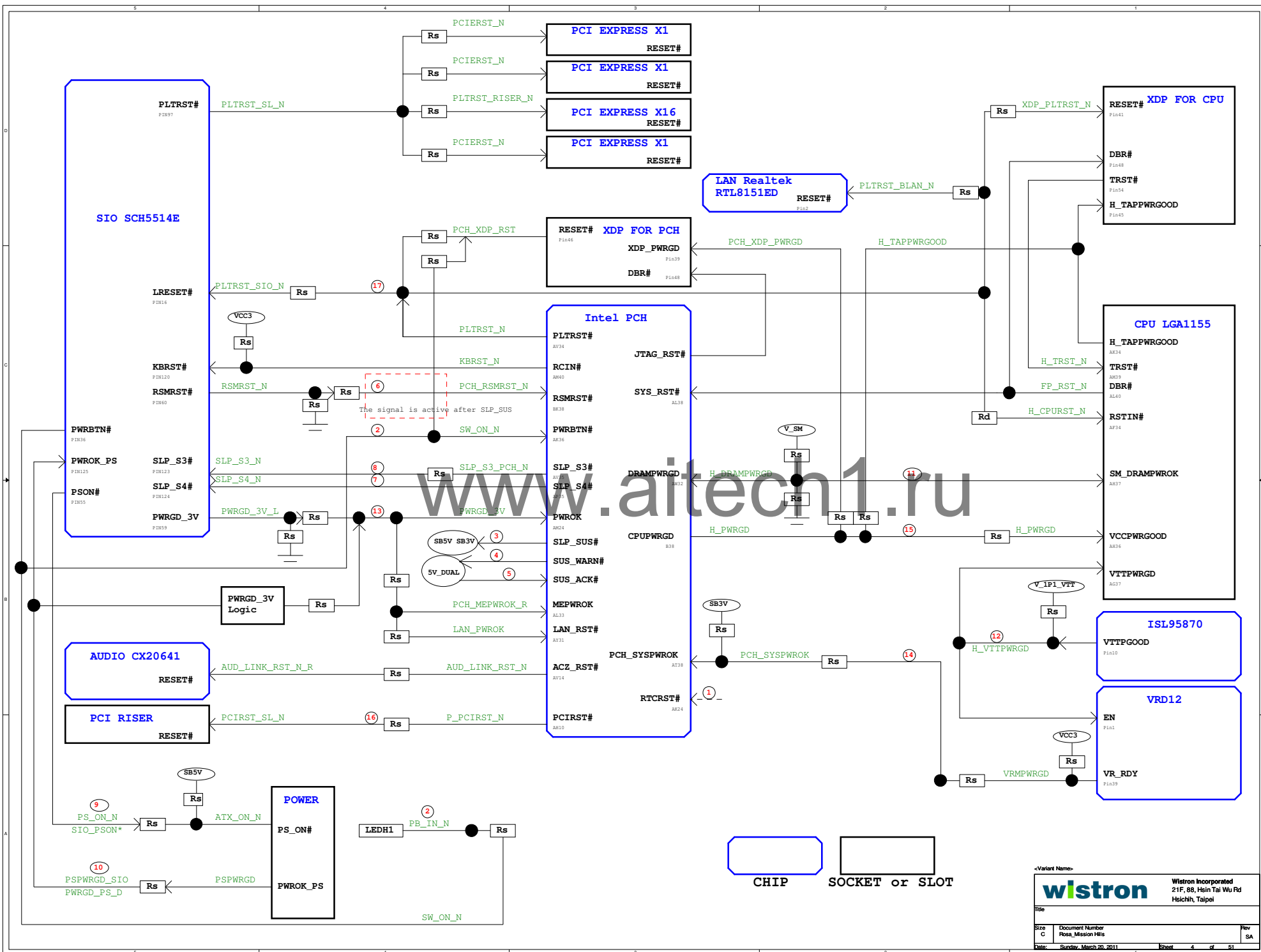
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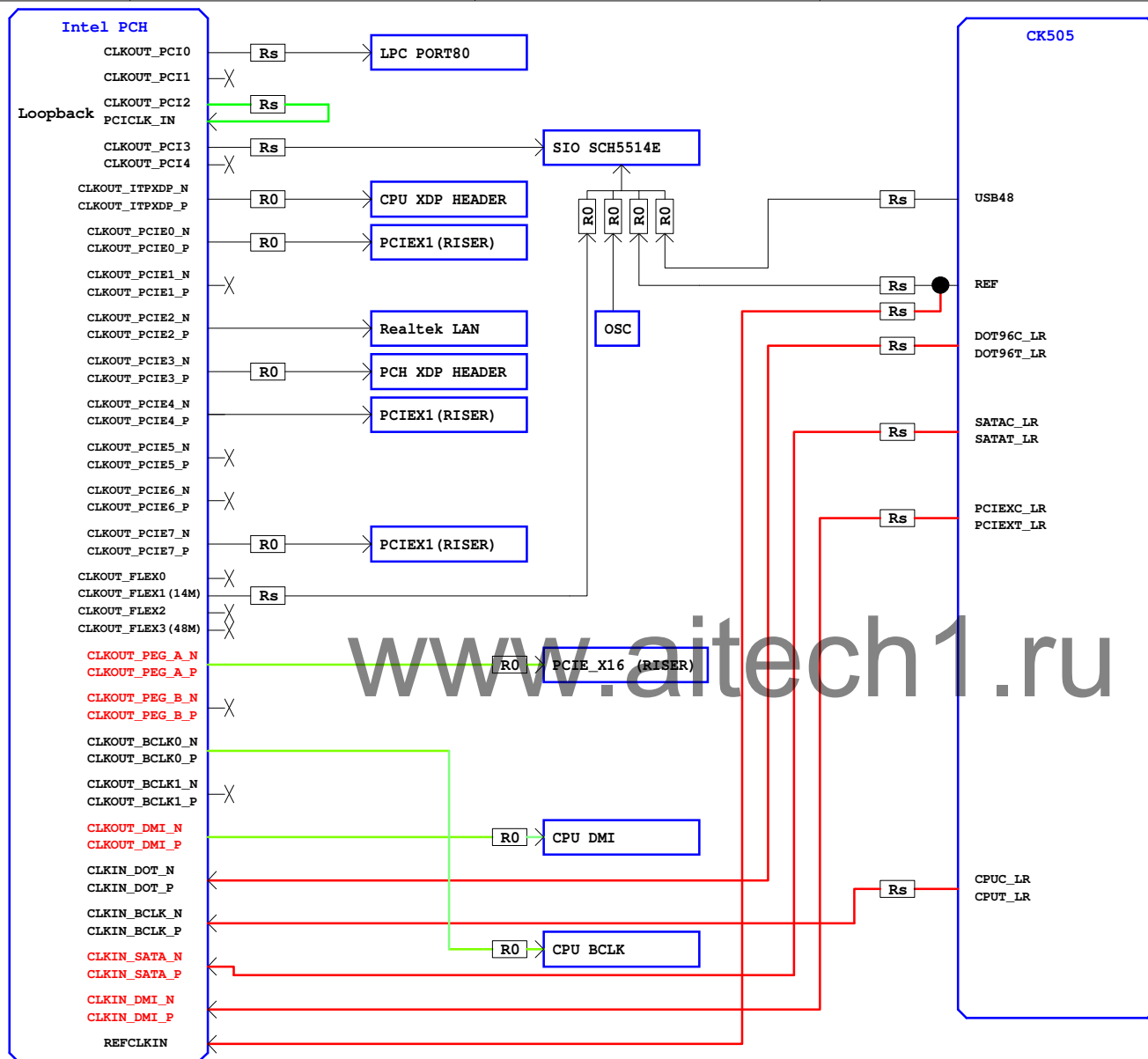
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Rev

SA





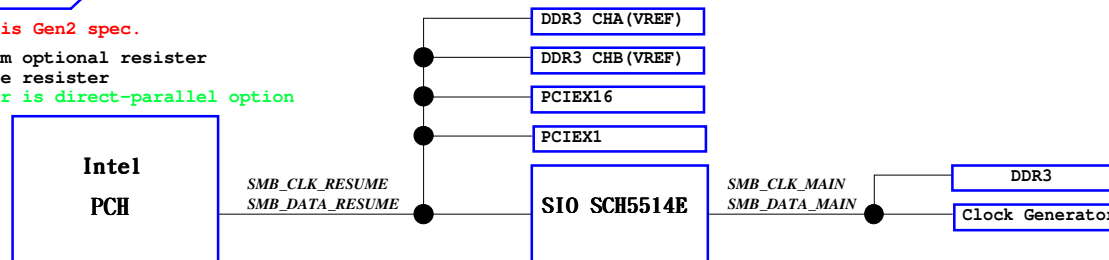
BTM: Buffer Through Mode
Need CK505 to provide 4 clock to PCH
FCIM: Full Clock Intergration Mode
Remove CK505

Note: Red Color is Gen2 spec.

Note: R0 is 0 ohm optional resistor

Note: Rs is serie resistor

Note: Green Color is direct-parallel option



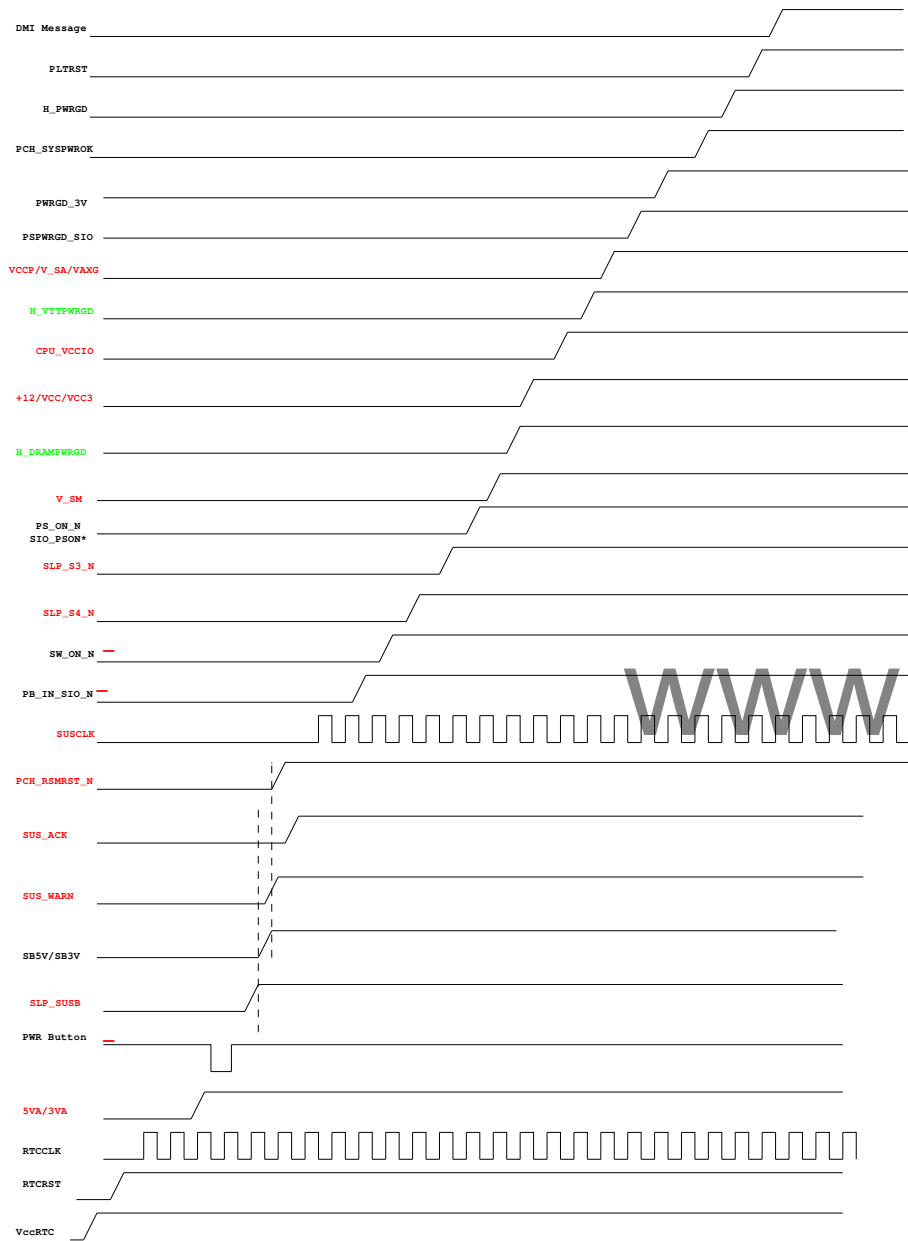
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POWER ON SEQUENCE



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PCH (H61)

PIN NAME	Pin#	POWER WELL	USAGE	BIO'S Post Value	Default Type	Notes
GPIO0	AW62	MAIN	PCD REQ_N	GPI (No Use)	GPI	10K P/U to VCC3 MAIN
GPIO1	BR19	MAIN	HDMI_DETECT	GPI (Low: NO HDMI, High: HDMI detect)	GPI	I P/U 20K
GPIO2	BN8	MAIN	P_INT_E_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO3	AV9	MAIN	P_INTF_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO4	BT15	MAIN	P_INTG_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO5	BR4	MAIN	P_INTH_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO6	BA22	MAIN	TACH2	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN, I P/U 20K
GPIO7	BR16	MAIN	TACH3	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN, I P/U 20K
GPIO8	BP51	RESUME	IO_SMI_N	GPI (IO, SMI, N)	GPO	10K P/U to SB3V
GPIO9	BJ41	RESUME	USB_OC5_R_N	NATIVE	Native	USB OVER CURRENT
GPIO10	BT45	RESUME	USB_OC6_R_N	NATIVE	Native	10K P/U to SB3V
GPIO11	BM49	RESUME	LPC_PME_N	GPI (LPC_PME_N)	Native	LPC_PME_N, 10K P/U to SB3V
GPIO12	BK50	RESUME	PCH_HEATSINK_DETECT (Reserved)	GPI (Low: PCH Heatsink detected, High: No PCH Heatsink)	Native	10K P/U to SB3V
GPIO13	BA25	RESUME	PWR_CLEAR	GPI (High: Normal, Low: Clear Password)	GPI	10K P/U to SB3V, With a Jumper to GND
GPIO14	BM45	RESUME	USB_OC7_R_N	NATIVE	Native	10K P/U to SB3V
GPIO15	BM55	RESUME	USB_OC7_R_N	GPO (Unused)	GPO	I P/U 20K (Strapping)
GPIO16	AU56	MAIN	FB_USB2F_DET	GPI (Low: Front USB detected, High: No Front USB)	GPI	10K P/U to VCC3 MAIN
GPIO17	BT17	MAIN	TACH0	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO19	AV52	MAIN	SATA1GP	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN (Strapping)
GPIO20	AV43	MAIN	BOARD_ID_0	GPI (No Use)	Native	10K P/U to VCC3 MAIN, 10K (R) P/U to GND
GPIO21	BC54	MAIN	FB_USB2F1_DET	GPI (Low: Card Reader detected, High: No Card Reader)	GPI	FB_USB2F1_DET, 10K P/U to VCC3 MAIN
GPIO22	BA53	MAIN	BIO5_RCY_GP22	GPI (No Use)	GPI	BIO5_RCY_GP22, 10K P/U to VCC3 MAIN
GPIO23	BA20	MAIN	LPC_DRQ1_N	GPI (Not required for test)	Native	Unused, I P/U 20K
GPIO24	BP53	RESUME	H_SKT0CC_R_N	GPI (Low: CPU detected, Floating: No CPU)	GPO	H_SKT0CC_R_N, 10K (R) P/U to +3P3V, AUX, 10K (R) P/U to GND
GPIO27	BJ43	ep Sleep Power W	PCH_GP27_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO28	BJ55	RESUME	PCH_GP28_PU	GPO (Unused)	GPO	10K (R) P/U to V_3P3_A
GPIO29	BM49	RESUME	SLP_LAN_N	GPO (S0/S5 Low, S3 High)	Native	LAN Enable/Disable
GPIO30	BU46	RESUME	SUS_WARNB	S5 Low to turn off LAN power in S5	GPI	Function Pin
GPIO31	BG43	ep Sleep Power W	PCH_GP31_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO32	BC56	MAIN	EXT_MUTEW	GPO (50 High, S3/S5 Low)	GPO	External Mute
GPIO33	BC25	MAIN	SOP_ENABLE_GP33	S3/S5 Low to mute external speaker	GPO	10K P/U to VCC3 MAIN
GPIO34	BL56	MAIN	SPK_DETECT	SPK_DETECT, 10K P/U to VCC3 MAIN	GPI	10K P/U to VCC3 MAIN
GPIO35	BJ57	MAIN	SPK_MUTEW	GPO (50 High, S3/S5 Low)	GPO	SPK_MUTEW, 10K P/U to VCC3 MAIN
GPIO36	BB55	MAIN	SATA2GP	GPI (Unused)	GPI	Unused, 10K (R) P/U to VCC3 MAIN
GPIO37	BB53	MAIN	SATA3GP	GPI (Unused)	GPI	Unused, 10K P/U to VCC3 MAIN
GPIO38	BE54	MAIN	CHASSIS_ID_0	GPI (Pis refer to CHASSIS_ID table)	GPI	CHASSIS_ID_0, 10K P/U to VCC3 MAIN
GPIO39	BF55	MAIN	CHASSIS_ID_1	GPI (Pis refer to CHASSIS_ID table)	GPI	CHASSIS_ID_1, 10K P/U to VCC3 MAIN
GPIO40	BD41	RESUME	USB_OC1_R_N	Native (OC1W)	Native	USB OVER CURRENT
GPIO41	BG41	RESUME	USB_OC2_R_N	Native (OC2W)	Native	USB OVER CURRENT
GPIO42	BK43	RESUME	USB_OC3_R_N	Native (Unused)	Native	10K P/U to SB3V
GPIO43	BF43	RESUME	USB_OC4_R_N	Native (OC4W)	Native	USB OVER CURRENT
GPIO44	BL54	RESUME	LAN_EN	GPI (High: LAN enable, Low: LAN disable)	Native	10K P/U to SB3V, 10K (R) P/U to GND
GPIO45	AV44	RESUME	1_WATT_CTRL_1	GPO (S0/S5 High, S3 Low)	Native	1_WATT_CTRL_1, 10K P/U to SB3V, 10K (R) P/U to GND
GPIO46	BP55	RESUME	INTRU_DET	GPI (Low: Intruder Cable detected, High: No Intruder)	Native	INTRU_DET, 10K P/U to SB3V, 10K (R) P/U to GND
GPIO48	AW53	MAIN	MTST_ID	GPI (High: Slim Tower, Low: Mini Tower)	GPI	MTST_ID, 10K P/U to VCC3 MAIN
GPIO49	BA56	MAIN	VGA_DET	GPI (High: VGA detected, Low: No VGA)	GPI	VGA_DET, 10K P/U to VCC3 MAIN
GPIO50	BT5	MAIN	P_REQ_N1	Native (Unused)	Native	Function Pin, 8.2K P/U to VCC3 MAIN
GPIO51	AV8	MAIN	P_REQ_N1	Native (Unused)	Native	Strap Pin, 10K (R) P/U GND, I P/U 20K
GPIO52	BR8	MAIN	P_REQ_N2	Native (Unused)	Native	Function Pin, 8.2K P/U to VCC3 MAIN
GPIO53	BU12	MAIN	P_REQ_N2	Native (Unused)	Native	Strap Pin, 10K (R) P/U GND, I P/U 20K
GPIO54	AV11	MAIN	P_REQ_N3	Native (Unused)	Native	Function Pin, 8.2K P/U to VCC3 MAIN
GPIO55	BE2	MAIN	P_GNT_N3	Native (Unused)	Native	Strap Pin, 10K (R) P/U GND, I P/U 20K
GPIO57	BT53	RESUME	ME_CNTL	GPI (High: BIOS OK, Low: BIOS Error)	GPI	Unused, 10K (R) P/U to SB3V, 47K P/U GND
GPIO58	BJ46	RESUME	SMLCLK_PCH	Native (Unused)	Native	SMLCLK_PCH, 10K P/U to SB3V
GPIO59	BM43	RESUME	USB_OC0_R_N	Native	Native	USB OVER CURRENT
GPIO60	BU49	RESUME	SMLALERT_PCH	Native (Unused)	Native	SMLALERT_PCH, 2.2K P/U to SB3V
GPIO61	BM54	RESUME	SUS_STAT_N	Native	Native	W_DISABLE_N, 10K P/U (R) to SB3V
GPIO62	BA47	RESUME	SUSCLK	Native	Native	Unused, TP
GPIO63	BD50	RESUME	SLP_S5_N	Native	Native	Unused, TP
GPIO64	AT9	MAIN	Test point (CLKOUTFLEX0)	GPO (Unused)	Native	Unused, I P/U 20K
GPIO65	BA5	MAIN	CK_14M_FLEX	Native (14.318MHz CLK)	Native	14.318MHz CLK for SIO1 P/U 20K
GPIO66	AW5	MAIN	Test point (CLKOUTFLEX2)	GPO (Unused)	Native	Unused, I P/U 20K
GPIO67	BA2	MAIN	BOARD_ID_1	GPI (Reserved, Board ID Table)	Native	P/U 20K
GPIO68	BU16	MAIN	FP_DETECT (Palm Beach MT/DT Only)	GPI (Low: PWR cable detected, High: No PWR cable)	TBD	10K P/U to VCC3 MAIN
GPIO69	BM18	MAIN	TACH5	Unused	TBD	Unused, 10K P/U to VCC3 MAIN
GPIO70	BN17	MAIN	SERIAL_DETECT	GPI (Low: COM Port/KBMS detected, High: No COM/KBMS)	GPI	SERIAL_DETECT, 10K P/U to VCC3 MAIN
GPIO71	BP15	MAIN	FP_AUD_DETECT	GPI (Low: Front Audio detected, High: No Front Audio)	GPI	FP_AUD_DETECT, 10K P/U to VCC3 MAIN
GPIO72	AV46	RESUME	USB_PWR_CRL1	GPO (S0/S3 High, S5 Low) If board ID is 11 S3 High to turn on USB 5V, S5 Low to turn off USB 5V	GPO	USB_PWR_CRL1, 10K P/U to SB3V
GPIO74	BR46	RESUME	SML1ALERT_PCH	Native (Unused)	Native	SML1ALERT_PCH, 10K P/U to SB3V
GPIO75	BR46	RESUME	SML1DATA_PCH	Native (Unused)	Native	SML1DATA_PCH, 10K P/U to SB3V

SCH5514E

GPIO#	Mux Function	GPIO Function	BIO'S Post Value	BIO'S Default value	BIO'S output type	Pull up/down
GP8051_1	DDC_DATA_2P5V	DIAG_LED1	GPO	Unused, follow original function	GPIO	Open Drain
GP8051_2	DDC_CLK_5V	DIAG_LED3	GPO	Unused, follow original function	GPIO	Open Drain
GP8051_3	DDC_DATA_5V	DIAG_LED3	GPO	Unused, follow original function	GPIO	Open Drain
GP8051_4	DDC_CLK_2P5V	DIAG_LED4	GPO	Unused, follow original function	GPIO	Open Drain
GP8051_5	PWRBT1W	Unused	Native	follow original function	Native	Push Pull
GP8051_6	R1W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_7	CTS2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_8	DSR2W	SMLIDATA_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
GP8051_9	DCD2W	SMLICLK_PCH_SIO	GPO (H)	Unused, set as "GPO" to prevent floating	GPIO	Push Pull
3P8051_10	DCD1W	Unused	Native	follow original function	Native	Input
3P8051_11	DSR1W	Unused	Native	follow original function	Native	Input
3P8051_12	RXD1	Unused	Native	follow original function	Native	Input
3P8051_14	TXD1	Unused	Native	follow original function	Native	Push Pull
3P8051_15	CTS1W	Unused	Native	follow original function	Native	Input
3P8051_16	DSR1W	Unused	Native	follow original function	Native	Push Pull
3P8051_17	R1W	Unused	Native	follow original function	Native	Input
GP10	SLP_S3W	Unused	Native	follow original function	Native	Push Pull
GP11	SLP_S5W	Unused	Native	follow original function	Native	Push Pull
GP14	HD_LEDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP21	P16IO31W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP22	P12/MRT1W/SCSW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP23	LATCHED_BF_CUT	Unused	Native	follow original function	Native	Push Pull
GP25	SCLK	Unused	Native	follow original function	Native	Open Drain
GP26	SCLK_1	Unused	Native	follow original function	Native	Open Drain
GP31	SECONDARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP33	PRIMARY_HDW	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP35	SDATLE1	Unused	Native	follow original function	Native	Open Drain
GP36	KBORSTW	Unused	Native	follow original function	Native	Open Drain
GP37	A20GATE	Unused	Native	follow original function	Native	Open Drain
GP40	DRIVEN0	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP41	IO_PMEW	Unused	Native	follow original function	GPIO	Open Drain
GP42	SDAT_1YD_SMIW	Unused	Native	follow original function	Native	Open Drain
GP52	RYD2	SLOTDC_N	Native	reserve, follow original function	GPIO	Push Pull
GP53	TXD2	COPEN_N	Native	reserve, follow original function	GPIO	Push Pull
GP55	RTS2W/DORC	CPURST_IN	Native	reserve, follow original function	GPIO	Push Pull
GP57	DTX2W	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP60	YELLOW	Unused	Native	follow Power LED behavior function	Native	Open Drain
GP61	GREEN	Unused	Native	follow Power LED behavior function	Native	Open Drain
GP75	DE_RSTDRWVW	IO_SMI_N	GPO (IO_SMI)	set as "GPO" for SMI function	Native	Open Drain
GP76	PCI_RST_3YSW	Unused	Native	follow original function	Native	Push Pull
GP77	PCI_RST_SLT5W	Unused	Native	follow original function	Native	Push Pull
GP80	PS_ONW	Unused	Native	follow original function	Native	Open Drain
GP81	BACKFEED_OUTW	Unused	Native	follow original function	Native	Open Drain
GP82	None	Unused	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull
GP83	PWR_GOOD2V	Unused	Native	follow original function	Native	Push Pull
GP84	RSWPS1W	Unused	Native	follow original function	Native	Push Pull

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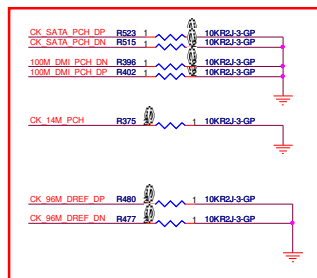
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PCH Buffer CLOCK

22 CK_96M_DREF_DP
22 CK_96M_DREF_DN
21 CK_SATA_PCH_DP
21 CK_SATA_PCH_DN
22 100M_DM1_PCH_DP
22 100M_DM1_PCH_DN

14M CLOCK

20 CK_14M_PCH



Terminate PCH CLK Inputs

Remove CLK GEN
Use PCH Internal CLK

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CLOCK

20 CK_PE_100M_MCP_DP
20 CK_PE_100M_MCP_DN

CPU_SA

VCCA_VID
49 VCCA_SENSE

CPU_VTT

49 VCCO_SEL
49 VCCO_SENSE
49 VSSO_SENSE

CPU_AXG

50 VCCO_SENSE
50 VSSO_SENSE

CPU_VCORE

50 VCCO_SENSE
50 VSSO_SENSE

ITP

14 H_TDO
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PROG_N
14 H_PRES_N

14 XDP_DBRESET_N
14 CK_XDP_S_DP
14 CK_XDP_S_DN

14 H_BPMM0
14 H_BPMM1
14 H_BPMM2
14 H_BPMM3
14 H_BPMM4
14 H_BPMM5
14 H_BPMM6
14 H_BPMM7

14.36 H_CPURST_N

OTHER

14.19.36 PLTRST_N
14.19 H_PWRGD
19 FP_RST_DBR_N
19.46 H_DRAMPWRGD
21.36 H_PECI
36.50 H_PROCHOT_N
21 H_THERMTRIP_N
19.56 H_SKT0CC_N
14.36 H_CPURST_N

23 H_SNB_N

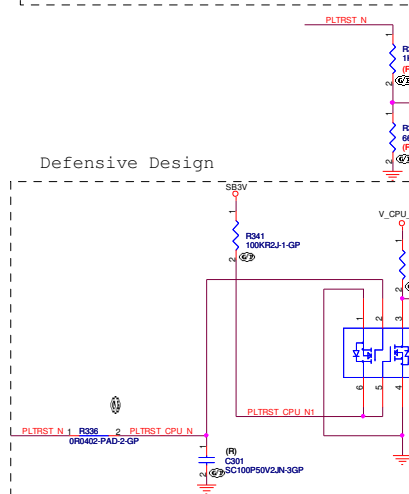
19.26.32.36.41 SMB_CLK_RESUME
19.26.32.36.41 SMB_DATA_RESUME

14 TPEV_SNB_PCODEBUG_0

03/21: follow CBI.0 out the CPU0 to XDP 1

MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SIM PAGE
PLACE IN CN3 AREA

H_VDSCK_VR R355 1 0P04 PAD-2-GP H_VDSCK
H_VDSOUT_VR R350 1 0P04 PAD-2-GP H_VDSOUT
H_VDALERT_N_VR R329 1 0P04 PAD-2-GP H_VDALERT_N



FDI

20 DL_FSYNC_0
20 DL_LSYNC_0
20 DL_FSYNC_1
20 DL_LSYNC_1
20 FDI_INT

20 FDI_TX_DP[0..7]
20 FDI_TX_DN[0..7]

PCIEX16

26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]

26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]

DMI

22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]

22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]

U27C

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EXP A RX DP0 B11
EXP A RX DN0 B12
EXP A RX DP1 D12
EXP A RX DN1 D11
EXP A RX DP2 C10
EXP A RX DN2 C9
EXP A RX DP3 E10
EXP A RX DN3 E9
EXP A RX DP4 B8
EXP A RX DN4 B7
EXP A RX DP5 C6
EXP A RX DN5 C5
EXP A RX DP6 A5
EXP A RX DN6 A6
EXP A RX DP7 E2
EXP A RX DN7 E1
EXP A RX DP8 F4
EXP A RX DN8 F3
EXP A RX DP9 G2
EXP A RX DN9 G1
EXP A RX DP10 H3
EXP A RX DN10 H4
EXP A RX DP11 J1
EXP A RX DN11 J2
EXP A RX DP12 K3
EXP A RX DN12 K4
EXP A RX DP13 L1
EXP A RX DN13 L2
EXP A RX DP14 M3
EXP A RX DN14 M4
EXP A RX DP15 N1
EXP A RX DN15 N2

DMI IT MR DP0 W5
DMI IT MR DN0 W4
DMI IT MR DP1 V3
DMI IT MR DN1 V4
DMI IT MR DP2 Y3
DMI IT MR DN2 Y4
DMI IT MR DP3 AA4
DMI IT MR DN3 AA5

P3
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DDR DATA

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17 M_DATA_B[0..63]
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15 M_DQS_A_DNP[0..8]
17 M_DQS_B_DP[0..8]
17 M_DQS_B_DNP[0..8]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]
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15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1
15 M_SCKE_A0
15 M_SCKE_A1
15 M_SCKE_B0
15 M_SCKE_B1
15 M_SCKE_B2
15 M_SCKE_B3

17 M_SCS_B_N0
17 M_SCS_B_N1
17 M_SCKE_B0
17 M_SCKE_B1
17 M_SCKE_B2
17 M_SCKE_B3

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DP
17 CK_M_DDR1_B_DN

DDR OTHERS

15,17 DDR3_DRAMRST_N

U27A

1 OF 11

M_MAA_A0 AW27 SA_MA_0
M_MAA_A1 AW24 SA_MA_1
M_MAA_A2 AW24 SA_MA_2
M_MAA_A3 AW23 SA_MA_3
M_MAA_A4 AW23 SA_MA_4
M_MAA_A5 AT24 SA_MA_5
M_MAA_A6 AT23 SA_MA_6
M_MAA_A7 AW22 SA_MA_7
M_MAA_A8 AW22 SA_MA_8
M_MAA_A9 AT22 SA_MA_9
M_MAA_A10 AW28 SA_MA_10
M_MAA_A11 AW21 SA_MA_11
M_MAA_A12 AT21 SA_MA_12
M_MAA_A13 AW22 SA_MA_13
M_MAA_A14 AW20 SA_MA_14
M_MAA_A15 AT20 SA_MA_15
M_WE_A_N AW23 SA_WE#
M_CAS_A_N AW20 SA_CAS#
M_RAS_A_N AW20 SA_RAS#
M_SBS_A0 AW29 SA_BS_0
M_SBS_A1 AW28 SA_BS_1
M_SBS_A2 AW20 SA_BS_2
M_SCS_A_N0 AW29 SA_CSF_0
M_SCS_A_N1 AW29 SA_CSF_1
M_SCKE_A0 AW19 SA_CKE_0
M_SCKE_A1 AW18 SA_CKE_1
M_SCKE_B0 AW18 SA_CKE_2
M_SCKE_B1 AW18 SA_CKE_3
M_ODT_A0 AW21 SA_ODT_0
M_ODT_A1 AW22 SA_ODT_1
M_ODT_B0 AW22 SA_ODT_2
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CK_M_DDR1_A_DP AW25 SA_CK_2
CK_M_DDR1_A_DN AW25 SA_CK_3
CK_M_DDR0_B_DP AW25 SA_CK_4
CK_M_DDR0_B_DN AW25 SA_CK_5
CK_M_DDR1_B_DP AW25 SA_CK_6
CK_M_DDR1_B_DN AW25 SA_CK_7

SM_DRAMRST#

OR0402-PAD-2-GP

SCDIU10V2K4-GP

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U27B

2 OF 11

M_MAA_B0 AK24 SB_MA_0
M_MAA_B1 AK20 SB_MA_1
M_MAA_B2 AK19 SB_MA_2
M_MAA_B3 AK18 SB_MA_3
M_MAA_B4 AK17 SB_MA_4
M_MAA_B5 AK16 SB_MA_5
M_MAA_B6 AK15 SB_MA_6
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M_MAA_B13 AK08 SB_MA_13
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M_MAA_B15 AK06 SB_MA_15
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M_CAS_B_N AK25 SB_CAS#
M_RAS_B_N AK24 SB_RAS#
M_SBS_B0 AP23 SB_BS_0
M_SBS_B1 AK22 SB_BS_1
M_SBS_B2 AW17 SB_BS_2
M_SCS_B_N0 AK25 SB_CSF_0
M_SCS_B_N1 AK25 SB_CSF_1
M_SCKE_B0 AU16 SB_CKE_0
M_SCKE_B1 AU15 SB_CKE_1
M_SCKE_B2 AU15 SB_CKE_2
M_SCKE_B3 AU15 SB_CKE_3
M_ODT_B0 AL26 SB_ODT_0
M_ODT_B1 AP25 SB_ODT_1
M_ODT_B2 AK26 SB_ODT_2
M_ODT_B3 AK26 SB_ODT_3
CK_M_DDR0_B_DP AL21 SB_CK_0
CK_M_DDR0_B_DN AL22 SB_CK_1
CK_M_DDR1_B_DP AL20 SB_CK_2
CK_M_DDR1_B_DN AK20 SB_CK_3
CK_M_DDR0_C_DP AL21 SB_CK_4
CK_M_DDR0_C_DN AL22 SB_CK_5
CK_M_DDR1_C_DP AL20 SB_CK_6
CK_M_DDR1_C_DN AK20 SB_CK_7

SM_DRAMRST#

OR0402-PAD-2-GP

SCDIU10V2K4-GP

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Can be left as no connects if no support ECC.

Can be left as no connects if no support ECC.

<Variant Name>

wlstron

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Title

Size

Document Number

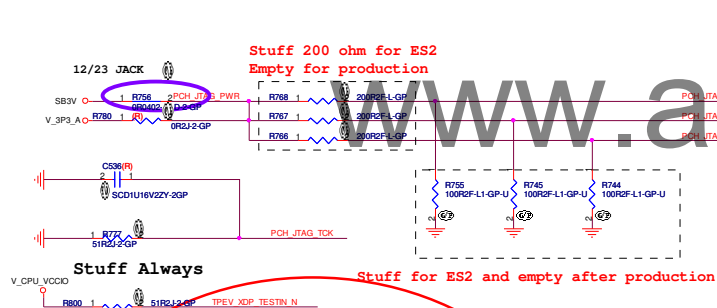
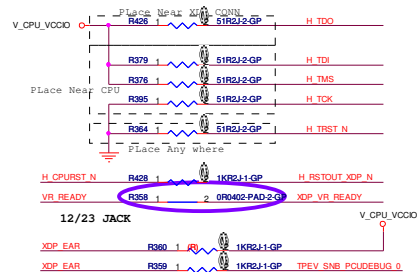
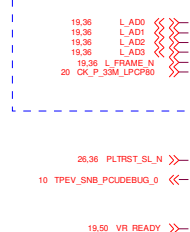
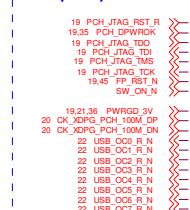
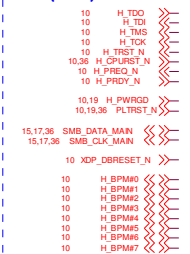
Posa_Mission Hills

New

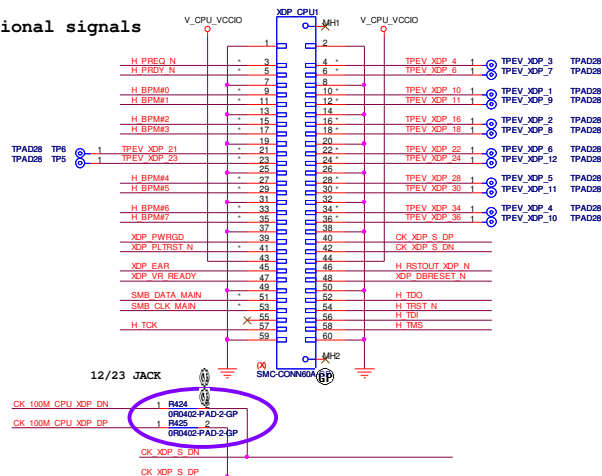
SA

Date: Sunday, March 20, 2011

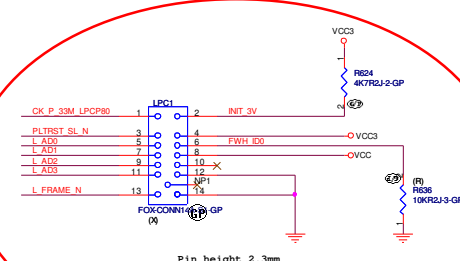
Sheet 12 of 51



~~All parts can be placed at back side~~



All parts can be placed at back side



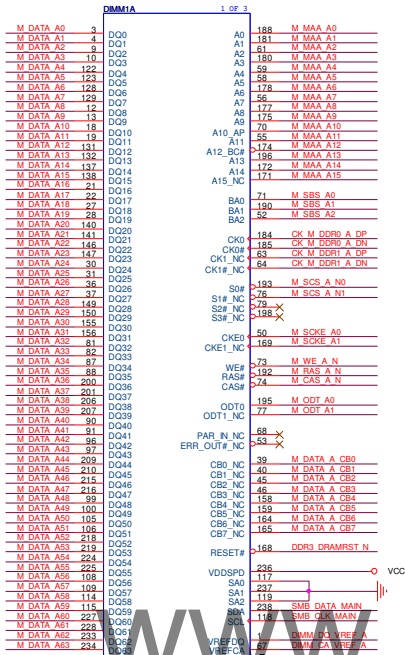
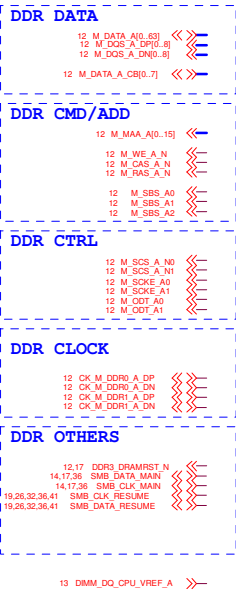
Pin height 2.3mm

Follow Eagle

<Variant Name>

Title

Size



Remove Channel A, DIMM1

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Size

C

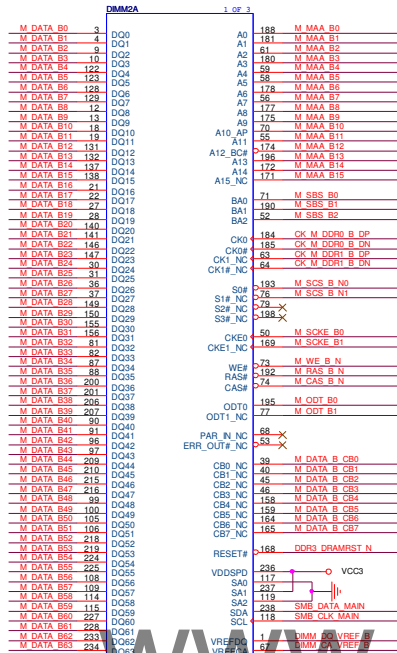
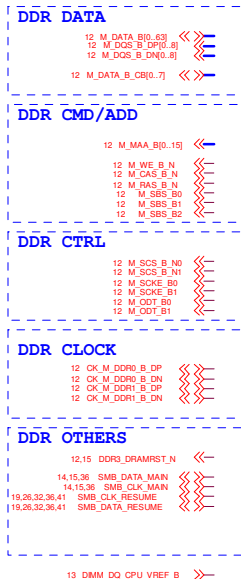
Document Number
Pesa_Mission Hills

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Remove Channel B, DIMM1

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<Variant Name>

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Title

Size

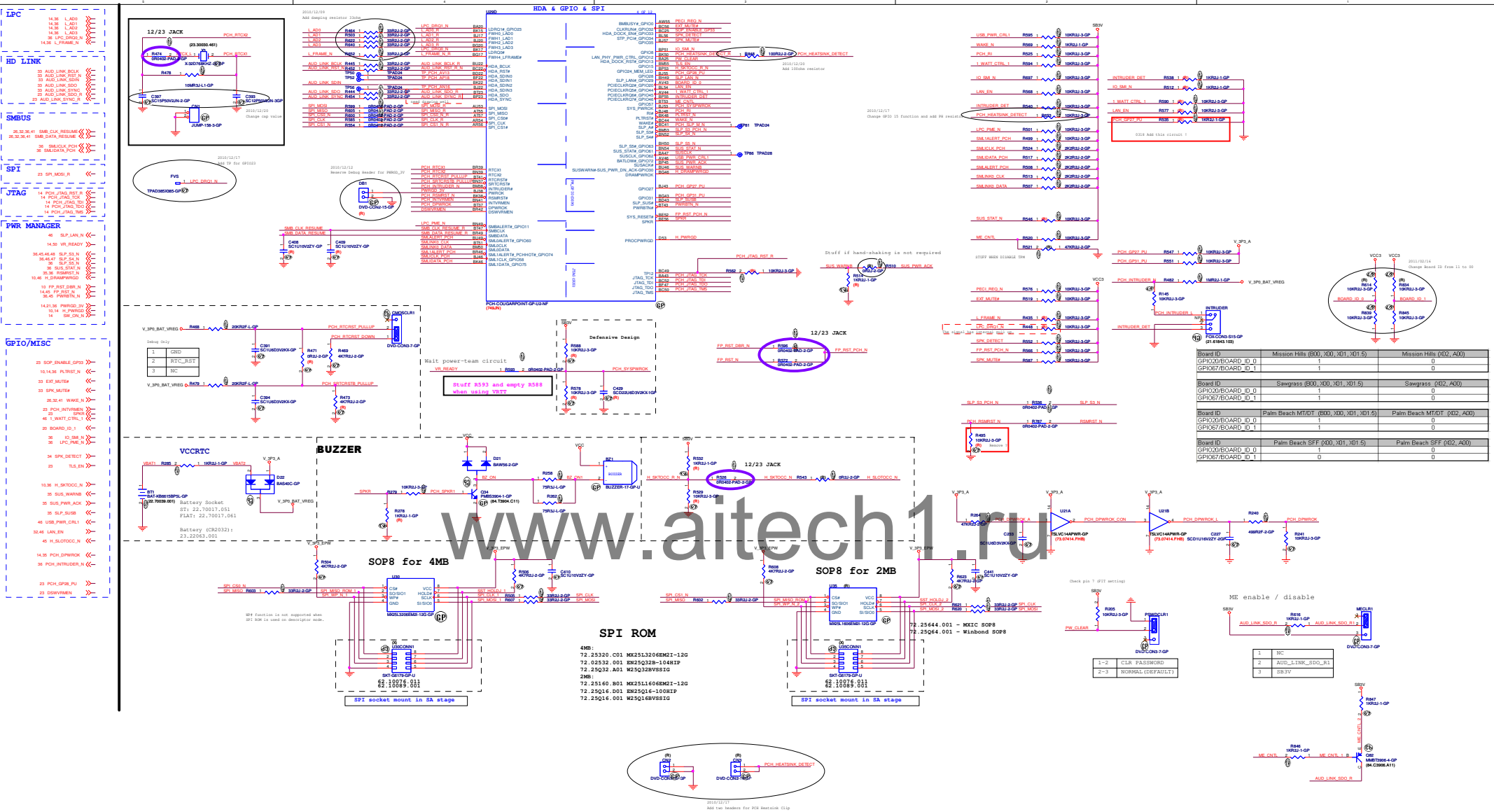
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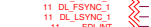
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GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

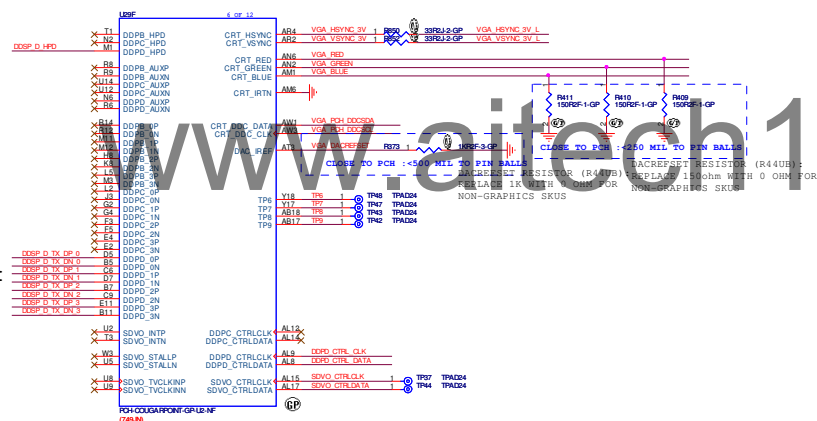
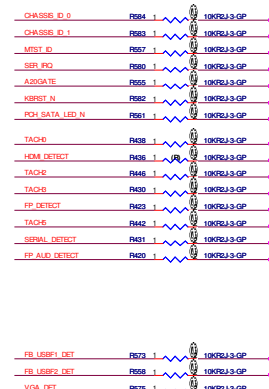
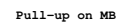
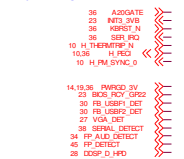
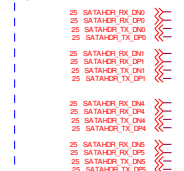
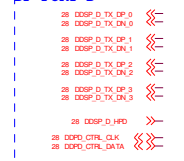
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GPIO67/BOARD_ID_1	1	0

Board ID	Palm Beach MT/OT (800_X00_X01_X01_2015)	Palm Beach MT/OT (800_X00_X01_X01_2015)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

Board ID	Palm Beach SFF (800_X00_X01_X01_2015)	Palm Beach SFF (800_X00_X01_X01_2015)
GPIO0/BOARD_ID_0	1	0
GPIO67/BOARD_ID_1	1	0

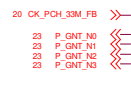
NVRAM





Port D: HDMI

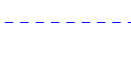
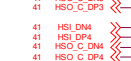
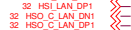
PCI



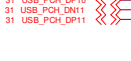
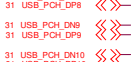
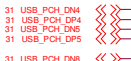
DMI



PCIE



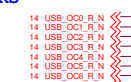
USB



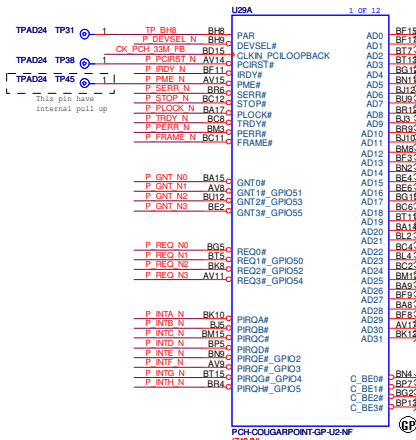
VGA_CLK



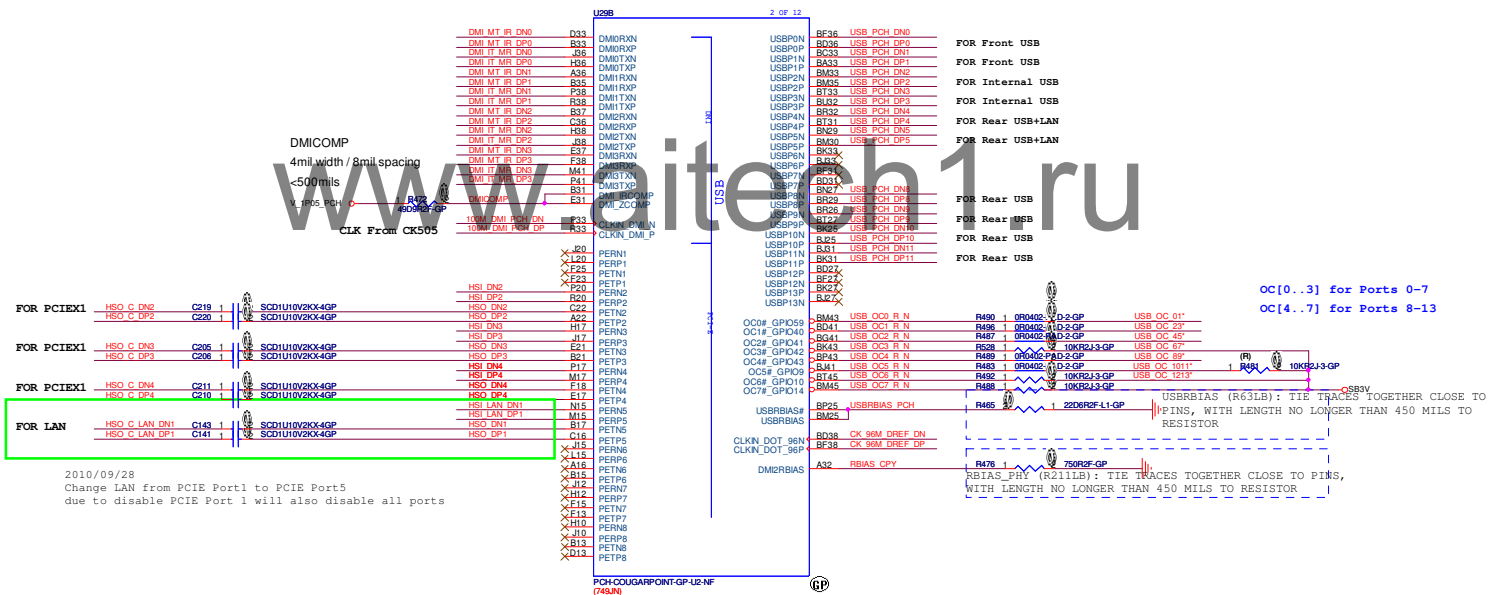
OTHERS



PCI



USB & DMI & PCIE



2010/09/28
Change LAN from PCIE Port1 to PCIE Port5
due to disable PCIE Port 1 will also disable all ports

<Variant Name>



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Title	Historian, Taipei
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BOOT DEVICE	GNT1	SATA1GP /GPIO19
SPI	1	1
PCI	1	0
FWH	0	0

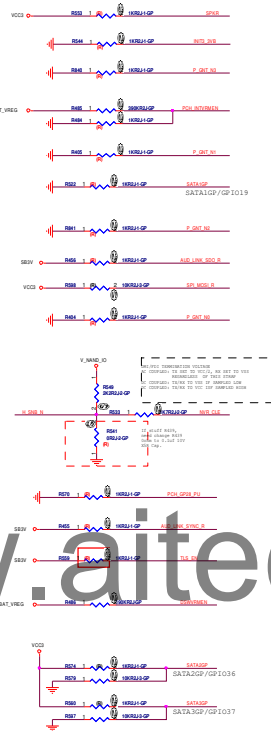


Table 2-27. Functional Strap Definitions (Sheet 1 of 5)

Table 2-27. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWRCK	The signal has a weak internal pull-down; hence the internal pull-down is disabled after PLTSTP is deasserted. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Chipset Board will disable the TCO timer; system-reboot feature). The status of this strap is readable via the NO_REBOOT bit (Chipset Config Register Offset: 2410h[Bit 5]).
		Falling edge of PWRCK	This signal has a weak internal pull-up; hence the internal pull-up is disabled after

Table 2-27. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GMT3# / OFI055	Top-Block Swap Override	During edge of PORC0	The signal takes a weak internal pull-up. Note: the internal pull-up is disabled after PLSTST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "topblock" swap mode. (Cousper Point assumes AS6 for all code targeting BIOS setup.) The status of this strap is available via Top-Swap Bit (C00F: Config Register Offset 0x44848). Note: that software can't be able to clear the Top-Swap Bit if the system is released without GMT3# being pulled down.
INTVMMEN	Integrated 1.25 VMM Probe / Disable	Always	Integrated 1.25 VMM is enabled when high. NOTE: This signal should always be high.

[illegible][illegible]

Table 2-27. Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment															
			This Signal has a weak internal pull-up. Note the internal pull-up is disabled if WRT0E desasserts. This field denotes the destination of accesses to the BSS memory range. Also controllable via the BSS Destination bit (Chapter Config registers). Offset: 0x00000020. This is used in conjunction with Boot BSS Destination Selection 1 strap.															
			<table><tr><th>RM11</th><th>RM10</th><th>Boot BSS06 Destination</th></tr><tr><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>IC1</td></tr><tr><td>1</td><td>1</td><td>SF1</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	RM11	RM10	Boot BSS06 Destination	0	1	Reserved	1	0	IC1	1	1	SF1	0	0	LPC
RM11	RM10	Boot BSS06 Destination																
0	1	Reserved																
1	0	IC1																
1	1	SF1																
0	0	LPC																
SATA0SP1 GPI0_19	Boot BSS05 Strap B1 0 44000	Pin edge of PwRCK																

6009								

Signal	Usage	When Sampled	Comment
HDA_SDO	Flash Descriptor Ownership / ID ME Debug Mode	Rising edge of RSTNTRST	Signal has a weak internal pull-down. If signal is sampled low, the security measures defined in the Flash- Descriptor will be in effect (default: If sampled low, Flash Descriptor Security will be disabled). This strap should only be asserted to external pull-up in manufacturing and test environments. RSTNTRST: The weak internal pull-down initiated after RSTNTRST deassertion. RSTNTRST: Asserting the HDA_SDO strap during edges of RSTNTRST will allow flash access. This strap should be brought up and disabled anytime IDMA features. This is a debug mode and will not be asserted after manufacturing.
DF_TVS	EMI and FEI TVS Rt. Terminator Voltage	Rising edge of PORTRST	This signal has a weak internal pull-up. RSTNTRST: The internal pull-up is disabled after RSTNTRST deassertion.

[illegible]

Table 2-27. Functional Strap Definitions (Sheet 5 of 5)

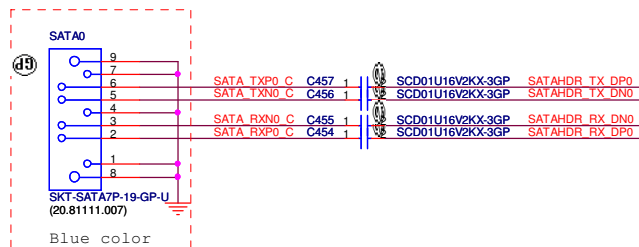
Signal	Usage	When Sampled	Comment
MOV_CTRLOA_T	Port A Detected	Rising edge of PACTCK	When "1", there is an internal pull-up resistor. If not detected, this signal may be an internal pull-up. NOTE: The manual pull-up does not affect the internal pull-up.
DEP_CTRLOA_T	Port C Detected	Rising edge of PACTCK	When "1", there is an internal pull-up resistor. If not detected, this signal may be an internal pull-up. NOTE: The manual pull-up does not affect the internal pull-up.
DOV_CTRLOA_T	Port D Detected	Rising edge of PACTCK	When "1", there is an internal pull-up resistor. If not detected, this signal may be an internal pull-up. NOTE: The manual pull-up does not affect the internal pull-up.
DOV_PVREN	Only Detects VDD1 VDD1 Low to High Regulator Enable	Always	If $\overline{VDD1}$ is sampled high, the internal pull-up resistor is enabled. If $\overline{VDD1}$ is sampled low, the internal pull-up resistor is disabled. NOTE: The manual pull-up does not affect the internal pull-up.
SAT5200/OWO36	Reserved	Rising edge of PACTCK	This signal may be an internal pull-up. NOTE: This signal should not be sampled when the chip is in sleep.
SAT5200/OWO17	Reserved	Rising edge of PACTCK	This signal may be an internal pull-up. NOTE: This signal should not be sampled when the chip is in sleep.

NOTE: See Section 2.1 for full details on sail-up/sail-down resistor



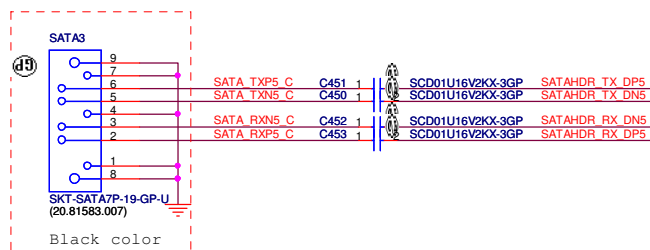
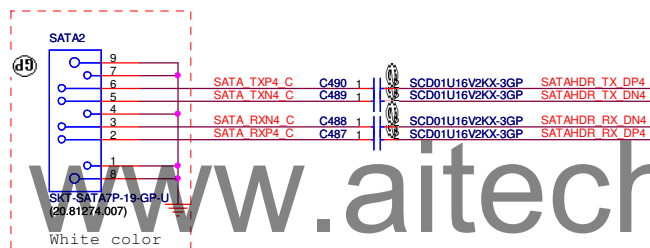
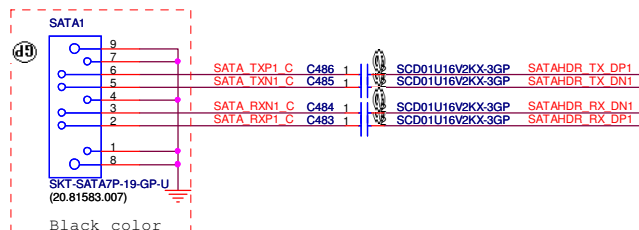
SATA

21 SATAHDR_RX_DP0 <<=
 21 SATAHDR_RX_DN0 >>=
 21 SATAHDR_TX_DN0 >>=
 21 SATAHDR_TX_DP0 <<=
 21 SATAHDR_RX_DP1 <<=
 21 SATAHDR_RX_DN1 >>=
 21 SATAHDR_TX_DN1 >>=
 21 SATAHDR_TX_DP1 <<=
 21 SATAHDR_RX_DP4 <<=
 21 SATAHDR_RX_DN4 >>=
 21 SATAHDR_TX_DN4 >>=
 21 SATAHDR_TX_DP4 <<=
 21 SATAHDR_RX_DP5 <<=
 21 SATAHDR_RX_DN5 >>=
 21 SATAHDR_TX_DN5 >>=
 21 SATAHDR_TX_DP5 <<=



NOTE:

PCH only port 0&1 support SATA 3.0



<Variant Name>

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Title

Size A3
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11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]

11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]

20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN

14,36 PLTRST SL_N

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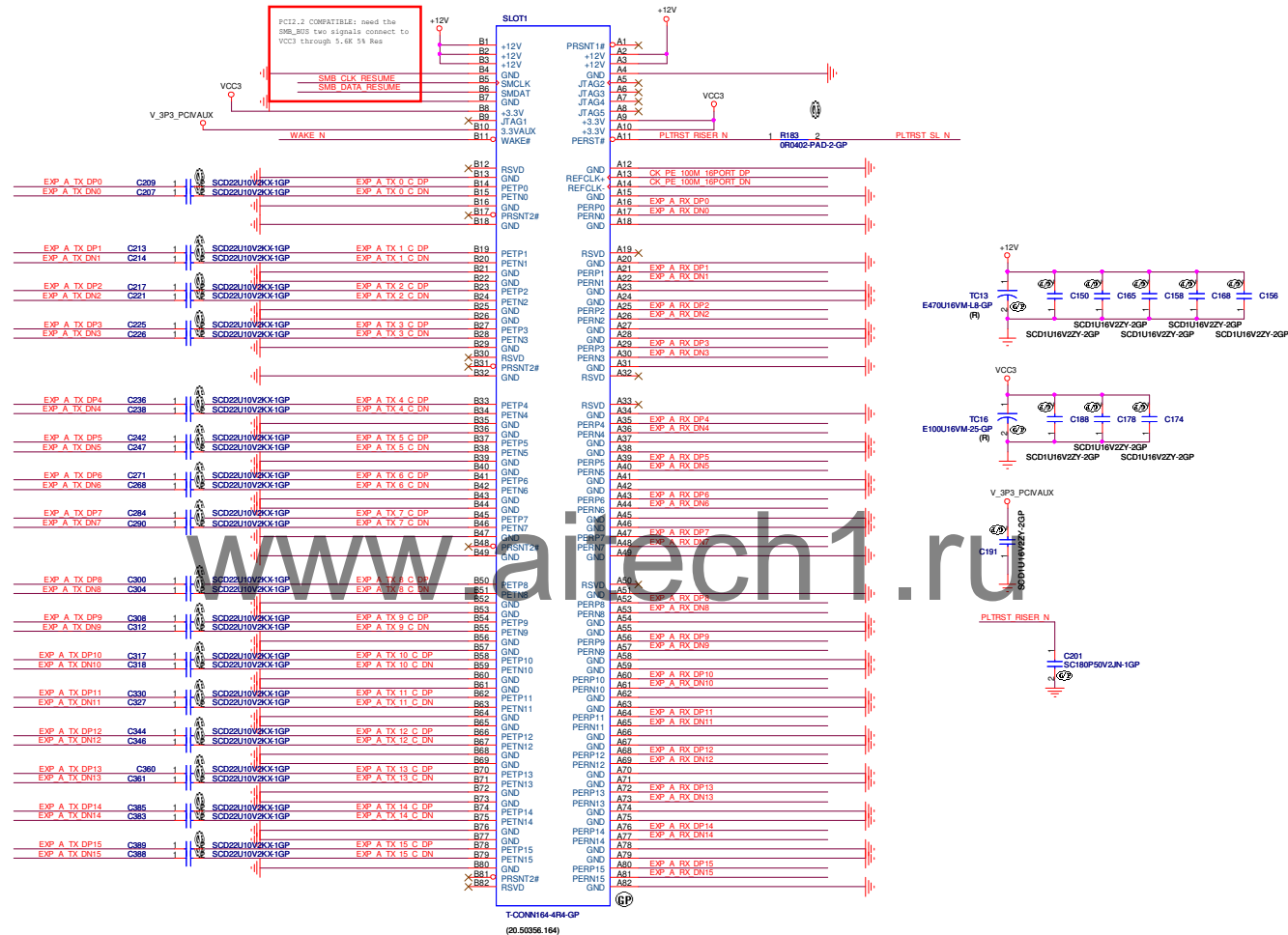
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19,32,36,41 SMB_CLK_RESUME  <<<>>>
19,32,36,41 SMB_DATA_RESUME  <<<>>>

19,32,41 WAKE_N <<>>

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PCIEx16 CONN may need LATCH if supporting 75W GFX Card



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RGB

21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE

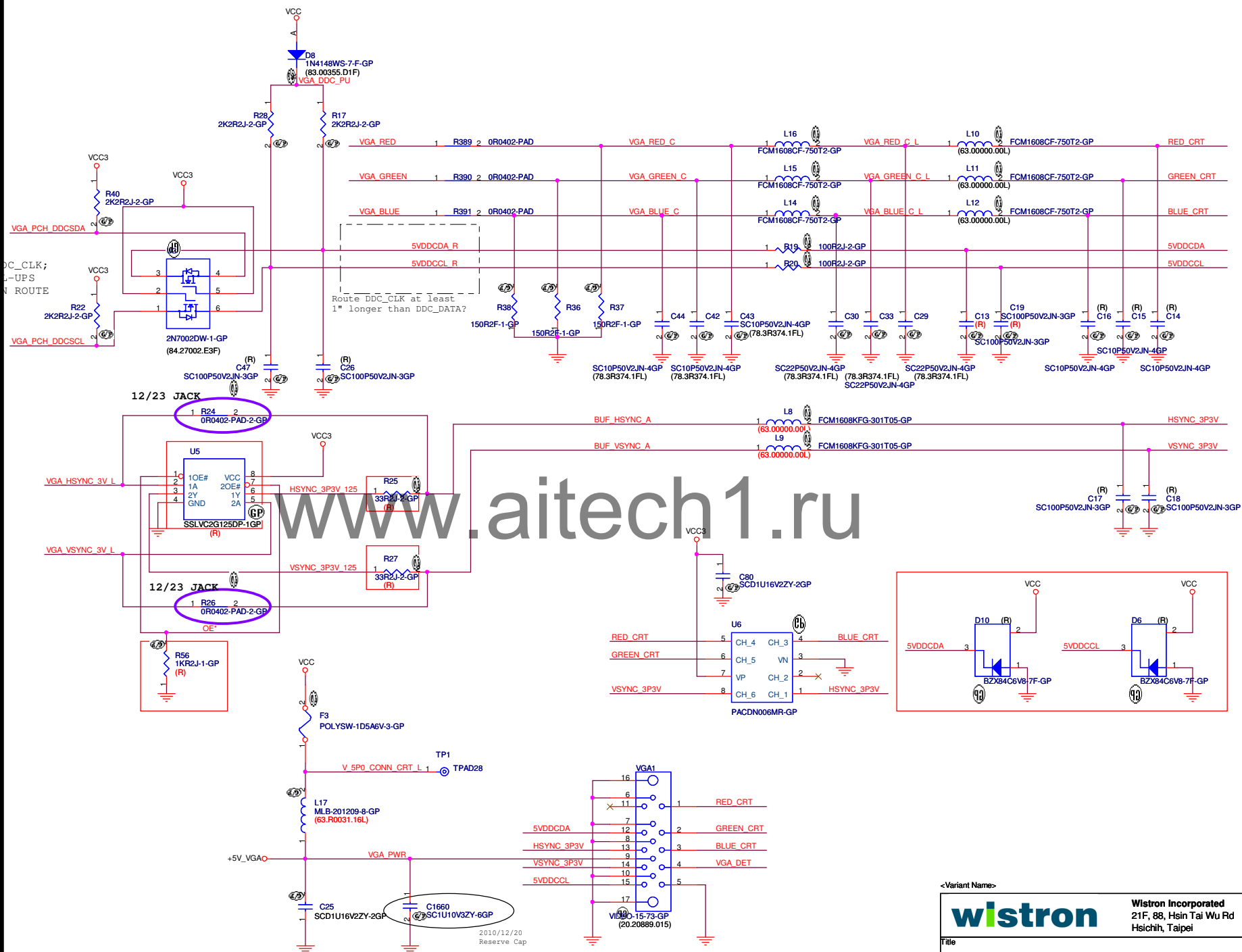
SYNC

21 VGA_HSYNC_3V_L
21 VGA_VSYNC_3V_L

DDC

21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
21 VGA_DET

DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE



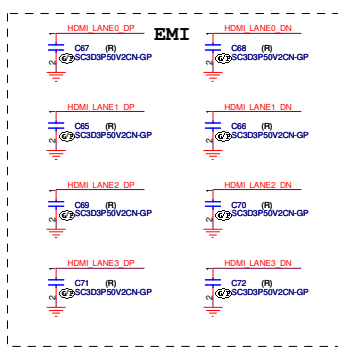
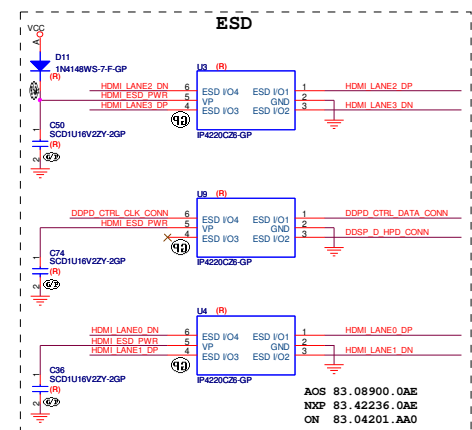
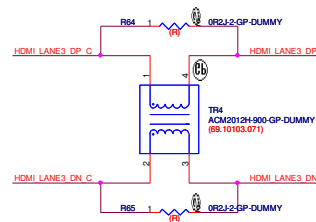
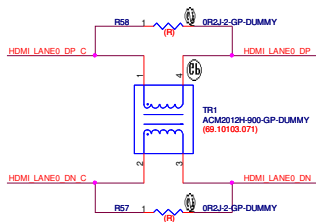
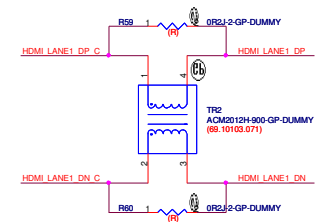
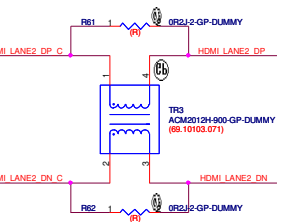
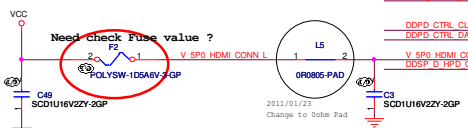
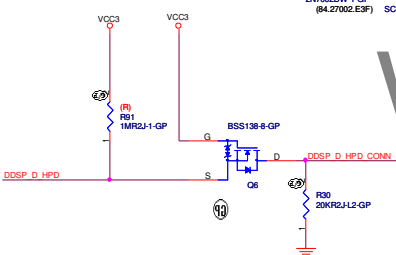
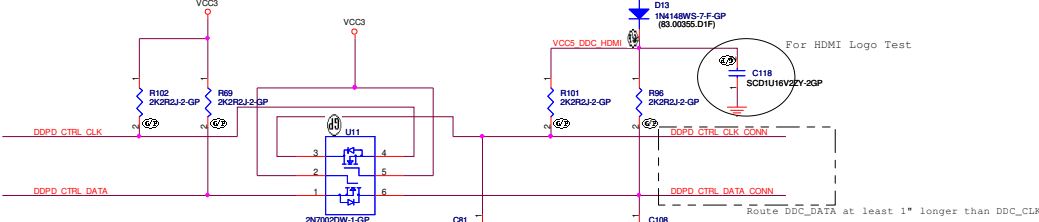
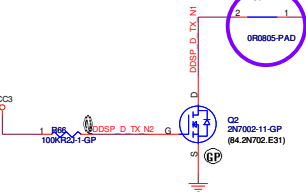
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DVI PORT

21 D0SP_D_TX_DP_0
21 D0SP_D_TX_DN_0
21 D0SP_D_TX_DP_1
21 D0SP_D_TX_DN_1
21 D0SP_D_TX_DP_2
21 D0SP_D_TX_DN_2
21 D0SP_D_TX_DP_3
21 D0SP_D_TX_DN_3
21 D0PD_CTRL_CLK
21 D0PD_CTRL_DATA
21 D0SP_D_HPD

PCH PORT D Place near HDMI Connector



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DISPLAY PORT

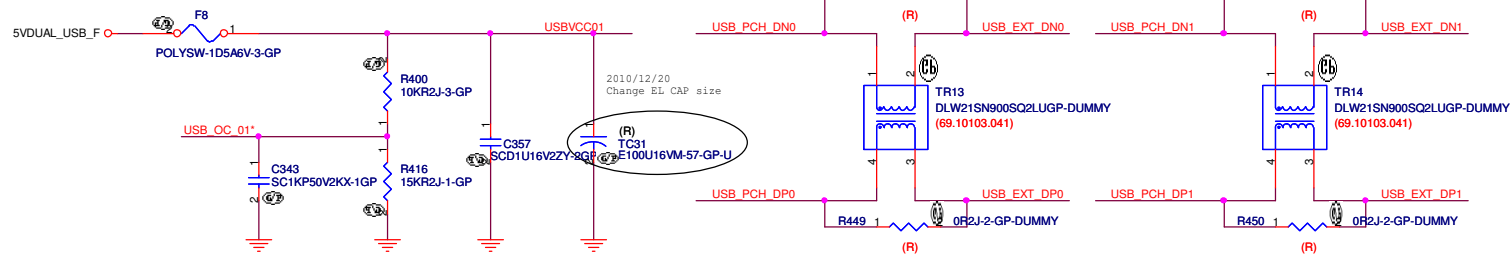
RESERVED

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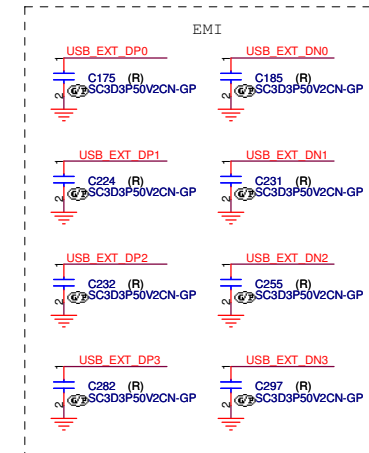
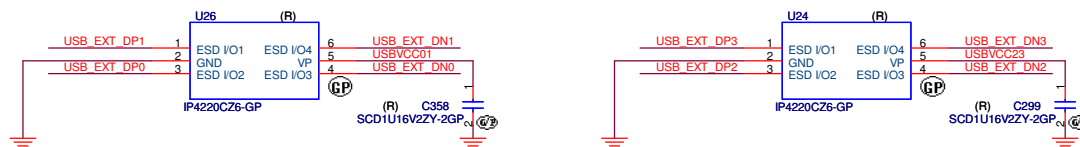
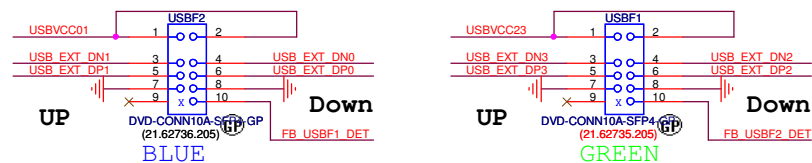
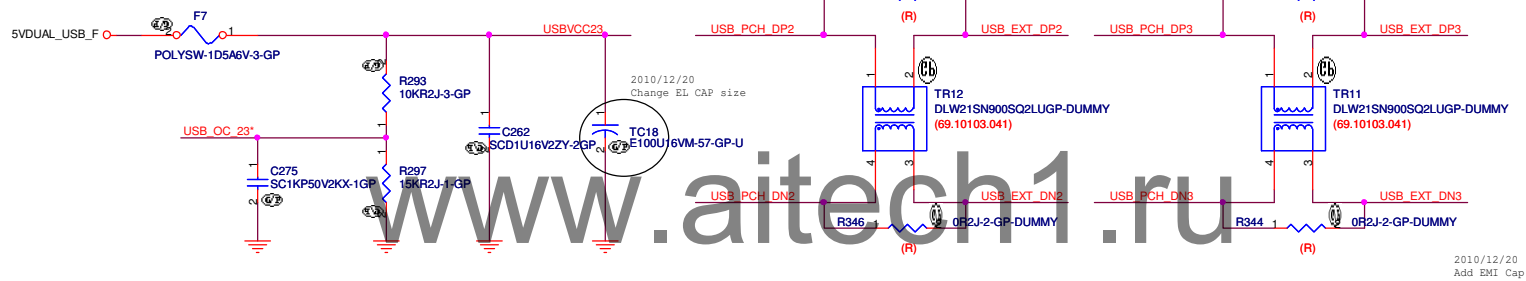
FRONT USB

- 22 USB_PCH_DP0
- 22 USB_PCH_DN0
- 22 USB_PCH_DP1
- 22 USB_PCH_DN1
- 22 USB_OC_01*
- 21 FB_USBF1_DET
- 22 USB_PCH_DP2
- 22 USB_PCH_DN2
- 22 USB_PCH_DP3
- 22 USB_PCH_DN3
- 22 USB_OC_23*
- 21 FB_USBF2_DET
- 22.31 USB_PCH_DN10
- 22.31 USB_PCH_DP10
- 22.31 USB_PCH_DN11
- 22.31 USB_PCH_DP11

FRONT USB PORT



FRONT USB PORT



REAR USB+LAN

```

22 USB_PCH_DP4
22 USB_PCH_DN4
22 USB_PCH_DNS
22 USB_PCH_DPS

32 LAN_MDIO2_DP
32 LAN_MDIO2_DN
32 LAN_MDIO1_DP
32 LAN_MDIO1_DN
32 LAN_MDIO0_DP
32 LAN_MDIO0_DN
32 LAN_MDIO3_DP
32 LAN_MDIO3_DN

32 SPEED_100_N
32 SPEED_1000_N

```

REAR USB

```

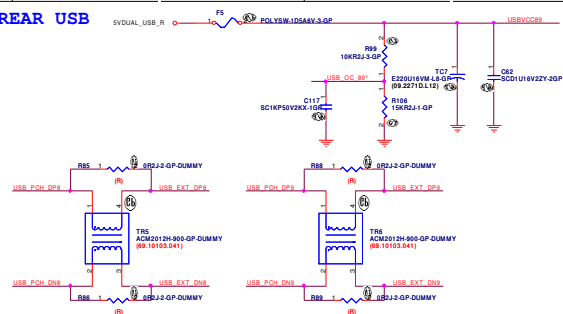
22 USB_PCH_DP8
22 USB_PCH_DN8
22 USB_PCH_DP9
22 USB_PCH_DN9

22 USB_PCH_DP10
22 USB_PCH_DN10
22 USB_PCH_DP11
22 USB_PCH_DN11

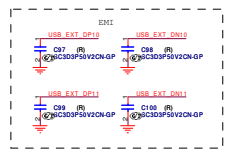
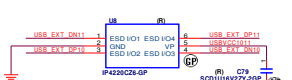
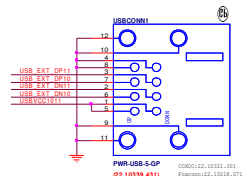
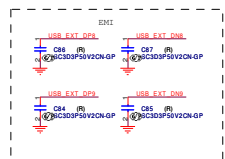
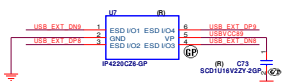
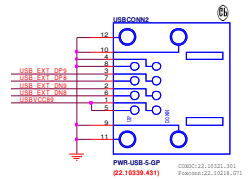
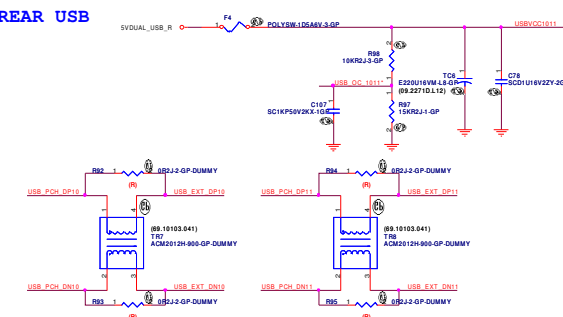
22 USB_OC_89*
22 USB_OC_45*

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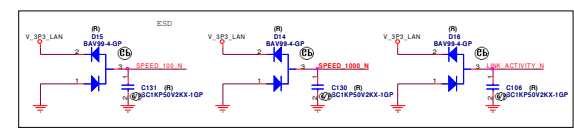
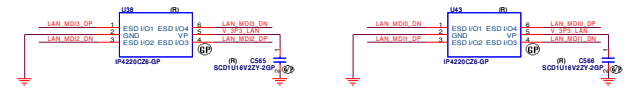
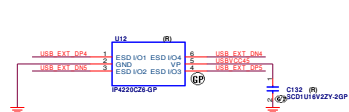
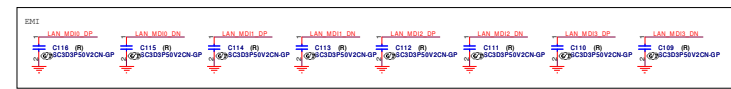
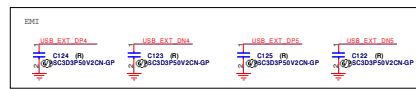
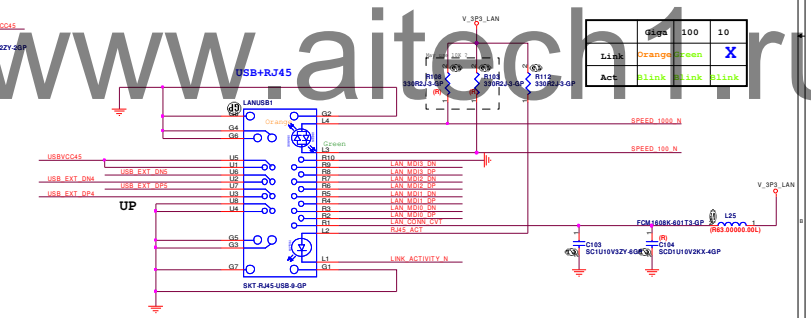
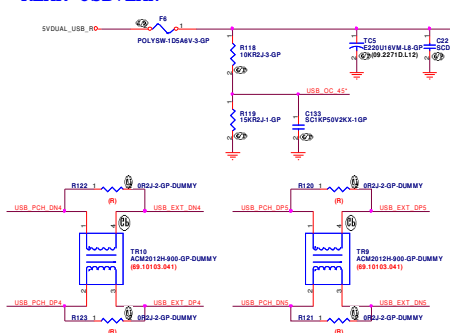
REAR USB



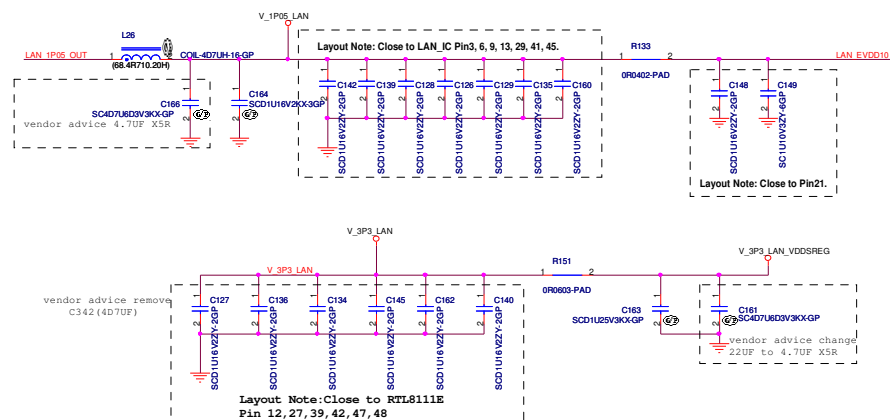
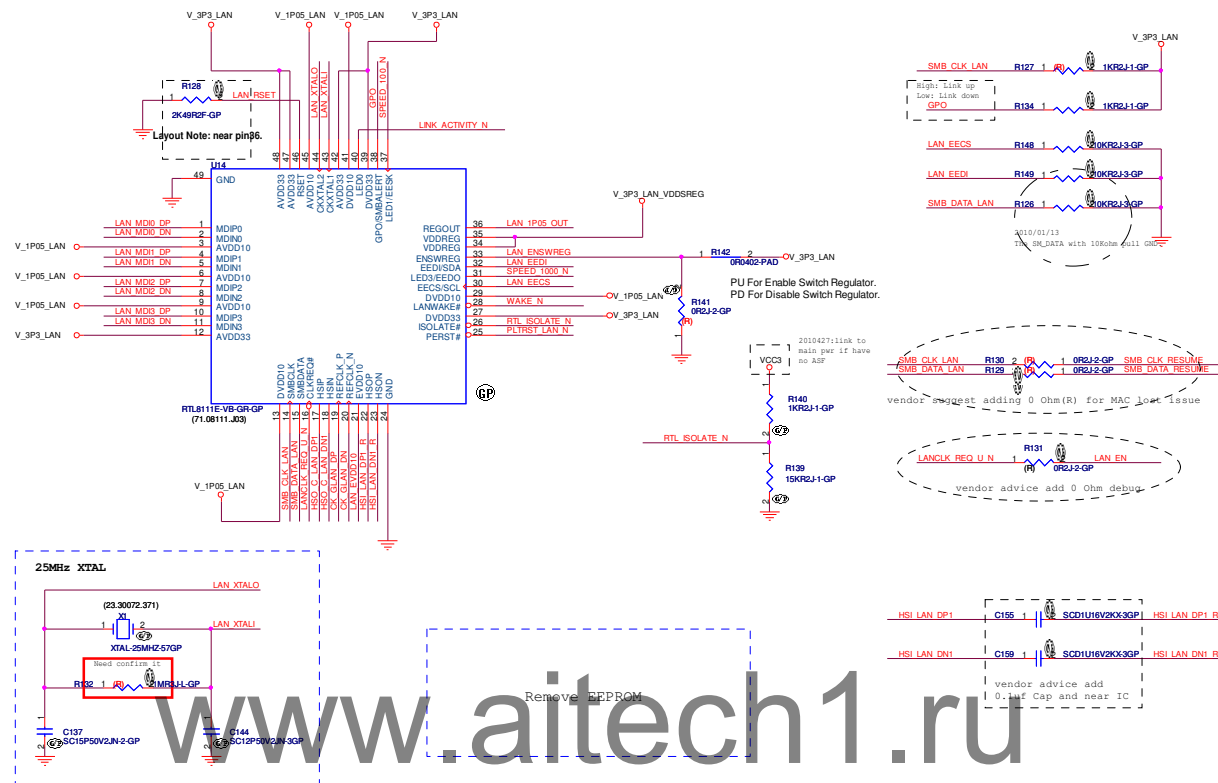
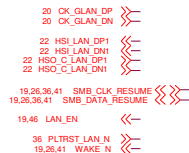
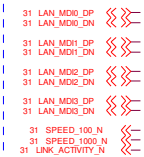
REAR USB



REAR USB+LAN



	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink



HD_LINK

19 AUD_LINK_SDN
19 AUD_LINK_SDO
19 AUD_LINK_RST_N
19 AUD_LINK_SYNC
19 AUD_LINK_BCLK

Rear I/O

LINE-OUT
34 LOUT_R
34 LOUT_L
34 LOUT_ID

LINE-IN
34 LIN_R
34 LIN_L
34 LIN_ID

MIC-IN
34 MIC_IN_R
34 MIC_IN_L
34 MIC_ID
34 MIC1_VREF0

Front I/O

HP-OUT
34 FP_OUT_L
34 FP_OUT_R
34 LINE2_ID

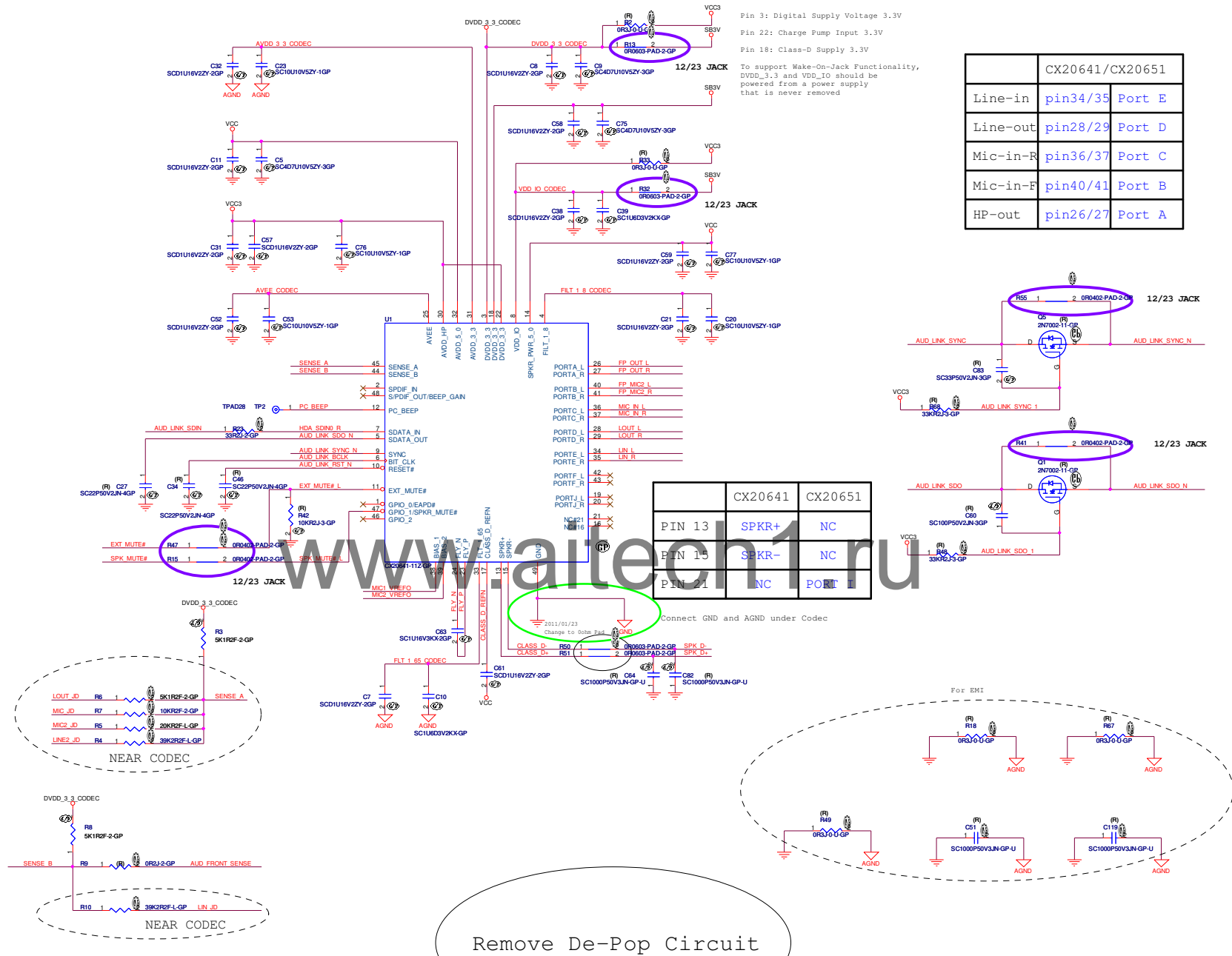
MIC-IN
34 FP_MIC2_R
34 FP_MIC2_L
34 MIC2_ID
34 MIC2_VREF0

Internal Speaker

34 SPK_D-
34 SPK_D+

Others

34 AUD_FRONT_SENSE
19 EXT_MUTE#
19 SPK_MUTE#



```

LINE-OUT
33      LOUT_R  >>>
33      LOUT_I  >>>
33      LOUT_D  >>>

LINE-IN
33      LIN_R   <<<
33      LIN_I   <<<
33      LIN_D   <<<

MIC-IN
33      MIC_IN_R <<<
33      MIC_IN_I <<<
33      MIC_D    <<<
33      MIC1_VREF0 <<<

```

```

HP-OUT
33  FP_OUT_R
33  FP_OUT_L
33  LINE2_JD

MIC-IN
33  FP_MIC2_R
33  FP_MIC2_L
33  MIC2_JD
33  MIC2_VREF0

```

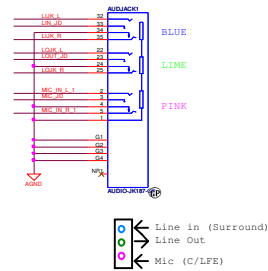
33	SPK_D-
33	SPK_D+
19	SPK_DETECT

```

30 AUD_FRONT_SENSE
21 FP_AUD_DETECT

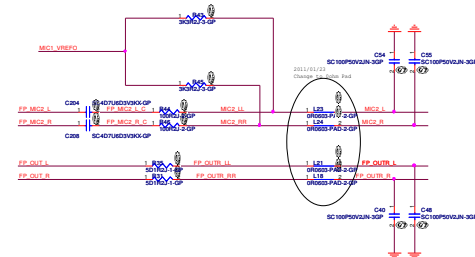
```

The schematic shows the internal wiring of the PCB near the connector. It includes signal traces for LIN_ID, LIN_V+, LIN_R, and LIN_GND. Key components include resistors R1 and R2, capacitors C37 and C45, and integrated circuits U1A and U1B. The layout is designed to ensure proper signal integrity and power distribution.

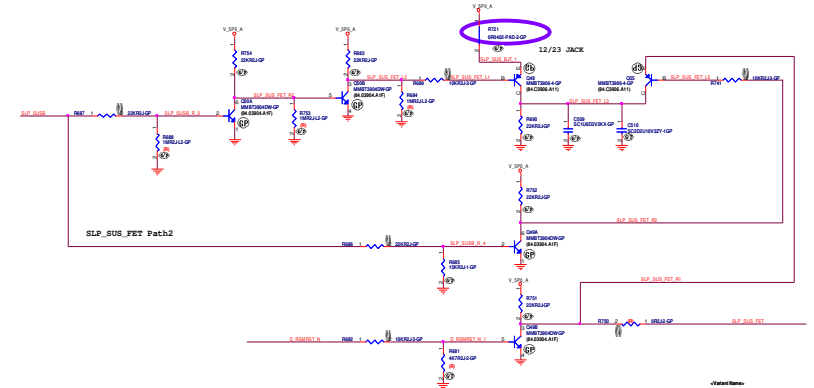
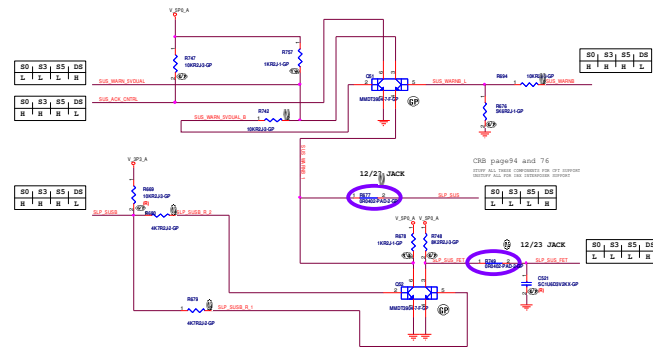
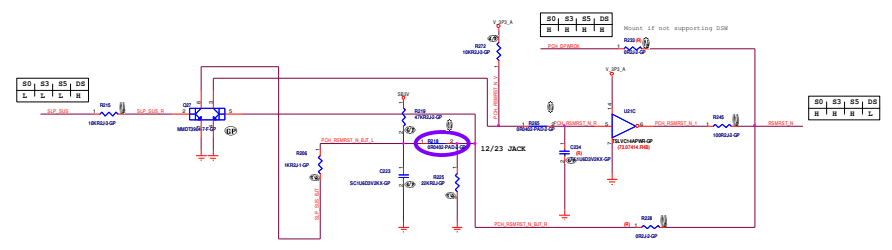
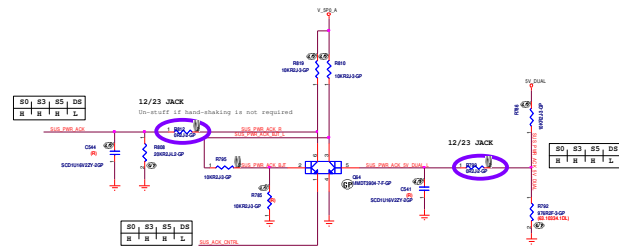
[illegible][illegible][illegible][illegible]

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Remove Mute Circuit

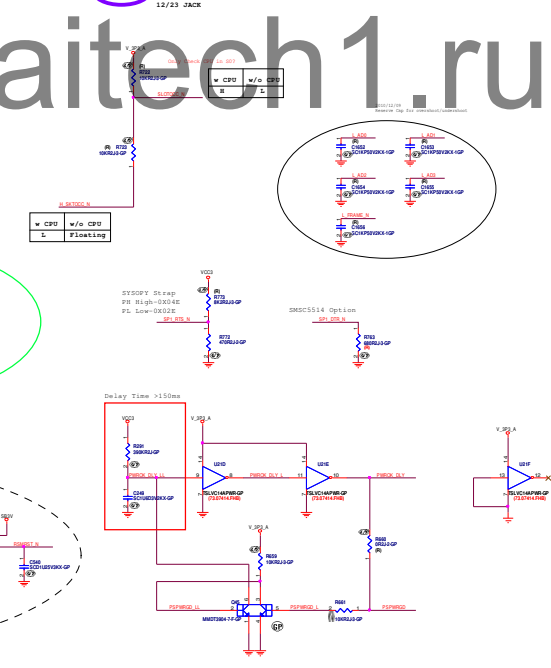
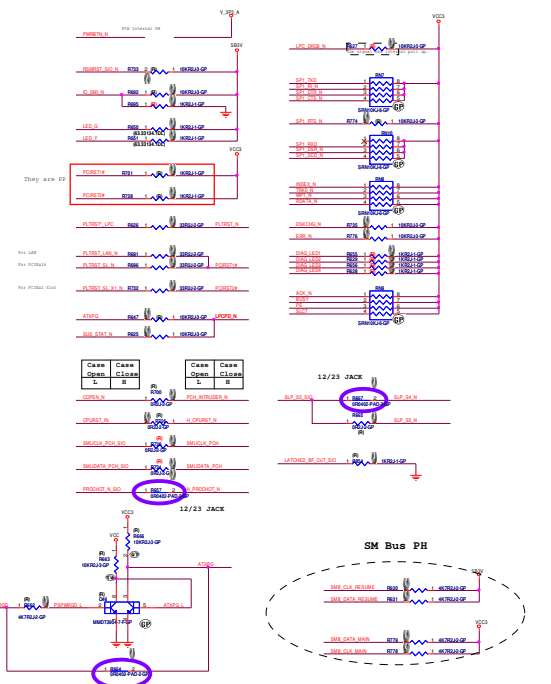
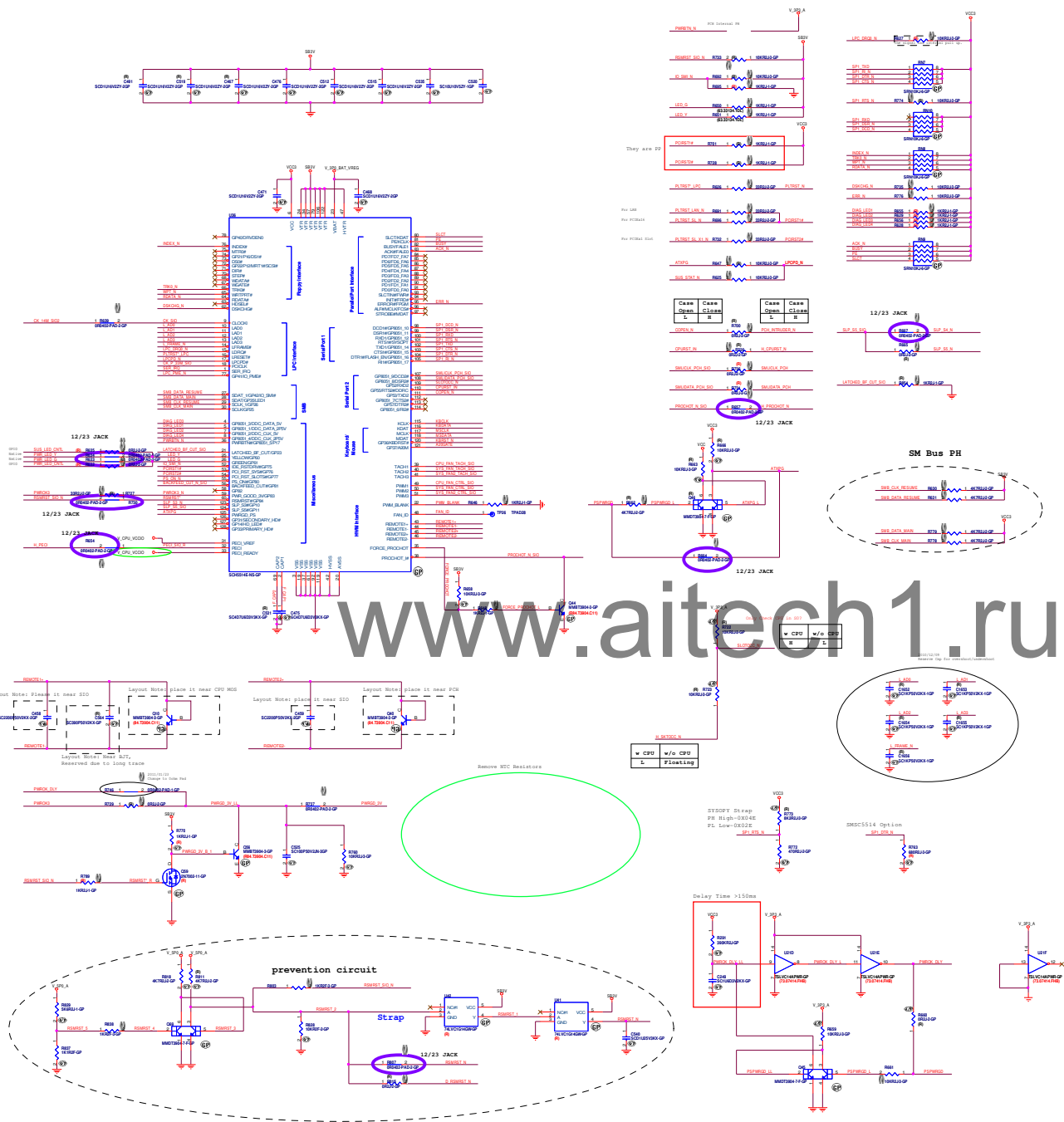


10 SUS_PWD_ACK
 10 SUS_WAKE
 10 SUS_BUSY
 40 SUS_BUSY_FET
 40 SUS_WAKE_SIGNAL
 1410 PWD_DISABLE
 1410 RSTWST_N
 50 R_POWERST_N



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FAN	14 FAN_PAN_TACH_S0	14 FAN_PAN_TACH_S0
CLOCK	14 CLK_14M_S0	14 CLK_14M_S0
LPC	14 LPC_14M_S0	14 LPC_14M_S0
COM	14 COM_14M_S0	14 COM_14M_S0
SMBUS	14 SMBUS_14M_S0	14 SMBUS_14M_S0
OTHERS	14 OTHERS_14M_S0	14 OTHERS_14M_S0
Power Manager	14 PM_14M_S0	14 PM_14M_S0
PECI	14 Peci_14M_S0	14 Peci_14M_S0
GPIO	14 GPIO_14M_S0	14 GPIO_14M_S0
KBMS	14 KBMS_14M_S0	14 KBMS_14M_S0
LED	14 LED_14M_S0	14 LED_14M_S0

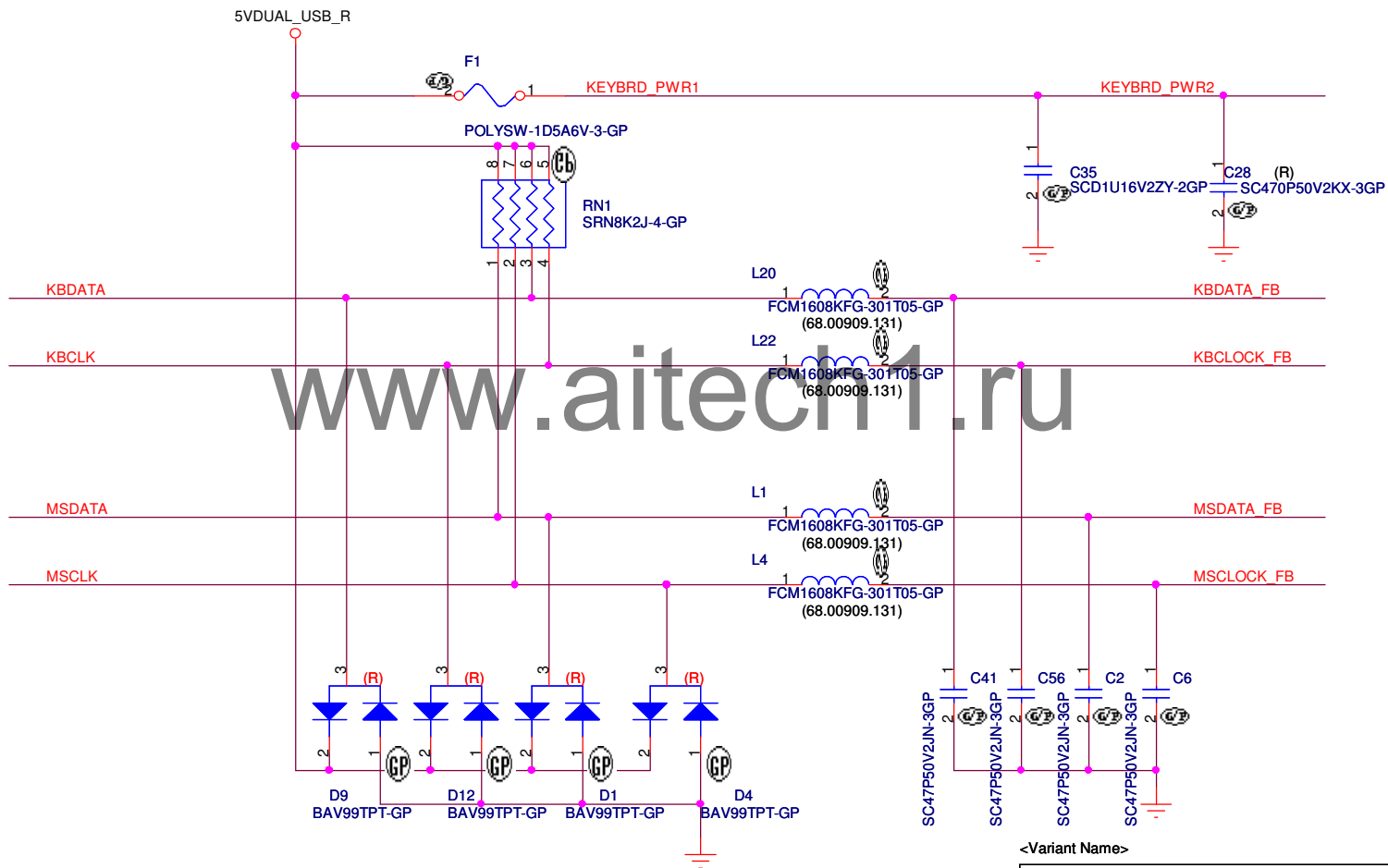


PS2 KB/MS

36 KBDATA <<>>
 36 KBCLK <<>>
 36 MSDATA <<>>
 36 MSCLK <<>>

38 KBDATA_FB <<>>
 38 KBCLOCK_FB <<>>
 38 MSDATA_FB <<>>
 38 MSCLOCK_FB <<>>

38 KEYBRD_PWR2 <<>>



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Size
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Document Number
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Rev
SA

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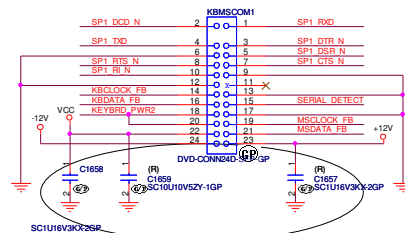
COM Port

36 SP1_RTS_N <<<
 36 SP1_DTR_N <<<
 36 SP1_DSR_N <<<
 36 SP1_RXD <<<
 36 SP1_DCD_N <<<
 36 SP1_TXD <<<
 36 SP1_CTS_N <<<
 36 SP1_RLN <<<

21 SERIAL_DETECT <<<

KB/MS

37 KBDATA_FB <<<
 37 KBCLK_FB <<<
 37 MSCLK_FB <<<
 37 KEYBRD_PWR2 >>>



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 Add cap for power noise

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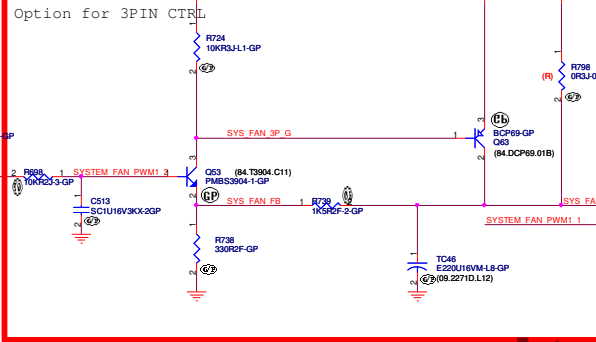
```
36 CPU_FAN_CTRL_SIO >>—
36 CPU_FAN_TACH_SIO <<—

36 SYS_FAN_CTRL_SIO >>—
36 SYS_FAN_TACH_SIO <<—

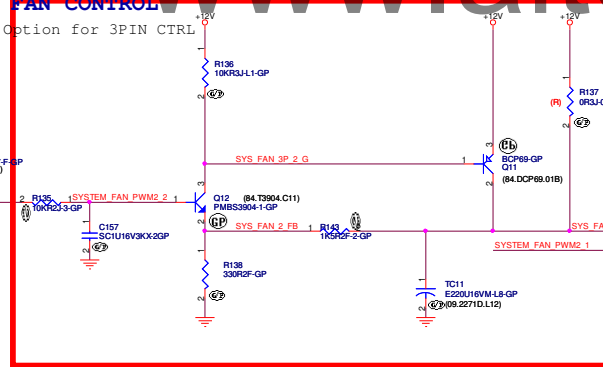
36 SYS_FAN2_CTRL_SIO >>—
36 SYS_FAN2_TACH_SIO <<—
```



Option for 3PIN CTRL



Option for 3PIN CTRL



Remove CPU Heatsink Screw Holes



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ONFI

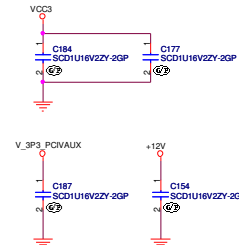
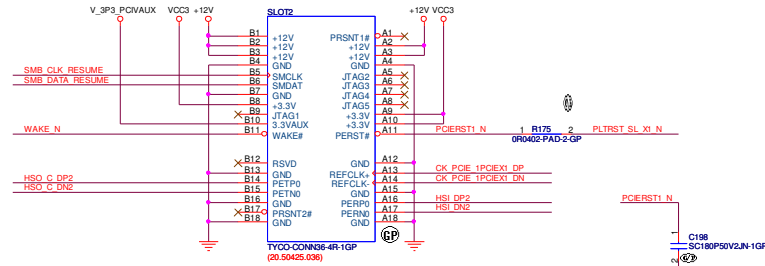
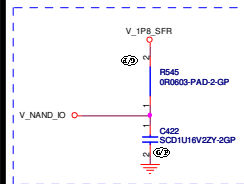
PCIEX1 CONN

PCIEX1

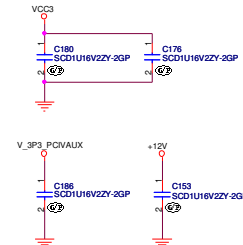
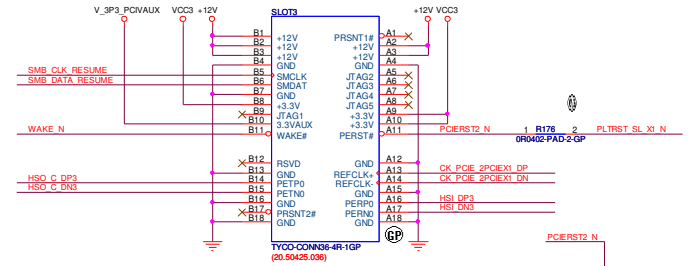
PCIEX1

PCIEX1

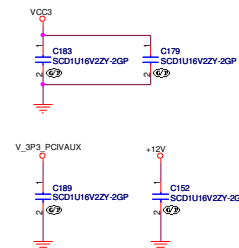
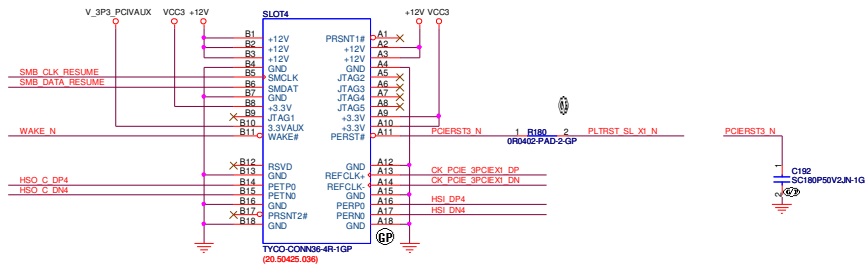
Others



PCIEX1 CONN



PCIEX1 CONN



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```

19  H_SLOT0CC_N      >>>
21  CHASSIS_ID_0     <<<
21  CHASSIS_ID_0     <<<
21  CHASSIS_ID_1     <<<
21  MTST_ID         <<<
21  FP_DETECT       <<<

36  PWR_LED_G       >>>
36  PWR_LED_Y       >>>

36  PWR_LED_CNTL    >>>
36  SUS_LED_CNTL    >>>

36  DIAG_LED1       >>>
36  DIAG_LED2       >>>
36  DIAG_LED3       >>>
36  DIAG_LED4       >>>

```

Prevent circuit

[illegible]

BIOS: Open-Drain
Default High, Output


The schematic diagram illustrates the LED driver circuit. It features two main power input sections at the top, both labeled V_5P0_A.

- Left Input Section:** A resistor R823 (330R3J-L-GP) is connected to the input. The signal path continues through a diode Q65 (PMES3904-1-GP) and a resistor R824 (330R3J-L-GP). This section is associated with the label PWR_LED_Y.
- Right Input Section:** A resistor R823 (330R3J-L-GP) is connected to the input. The signal path continues through a diode Q70 (PMES3906-GF) and a resistor R824 (330R3J-L-GP). This section is associated with the label SUS_LED_CNTL.

The output of the left section is connected to the PWR_LED_Y pin of the LED array. The output of the right section is connected to the SUS_LED_CNTL pin of the LED array. The LED array is represented by a symbol with multiple pins, including PWR_LED_Y, SUS_LED_CNTL, and others. The entire circuit is powered by a common ground connection at the bottom.

BIOS: Open-Drain
Default High, Output

DVD-CONN6D-SFP-GP

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Title				
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```

36.45 P5PWGRD >>
19.36.45.46 SLP_S3_N >>
19 1_WATT_CTRL_1 >>
19 SLP_LAN_N >>

5 LATCHED_BF_CUT_SIO >>
BACKFEED_CUT_N_SIO >>

10.19 H_DRAMPWRD >>
5 SUS_WARN_SVDUAL >>
19 USB_PWR_CRL1 >>
19.32 LAN_EN >>
19.36.46 SLP_S4_N >>

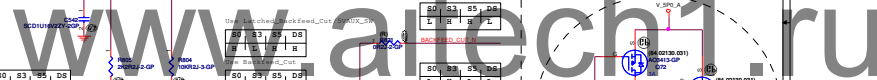
```



2010/12/22
Reserve die meer SPID t



Figure 1: Schematic diagram of the experimental setup. The top part shows a top-down view of a rectangular chip with three electrodes labeled S3, S5, and D5. The bottom part shows a cross-sectional view of the waveguide structure, with a red line representing the waveguide and a blue wavy line representing the surface plasmon wave. The waveguide is labeled 'CUT W' and 'R250'. A red dot is labeled 'R' and a blue dot is labeled 'R250'.



The diagram shows a 3-bit DAC circuit. It consists of three op-amp buffers (U1, U2, U3) configured as voltage followers. The inputs to the buffers are labeled D2, D1, and D0, which are connected to a 3-bit digital input. The outputs of the buffers are connected to a resistor network. The resistors are labeled R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100. The output of the circuit is labeled VOUT. The circuit is powered by a 5V supply and ground.

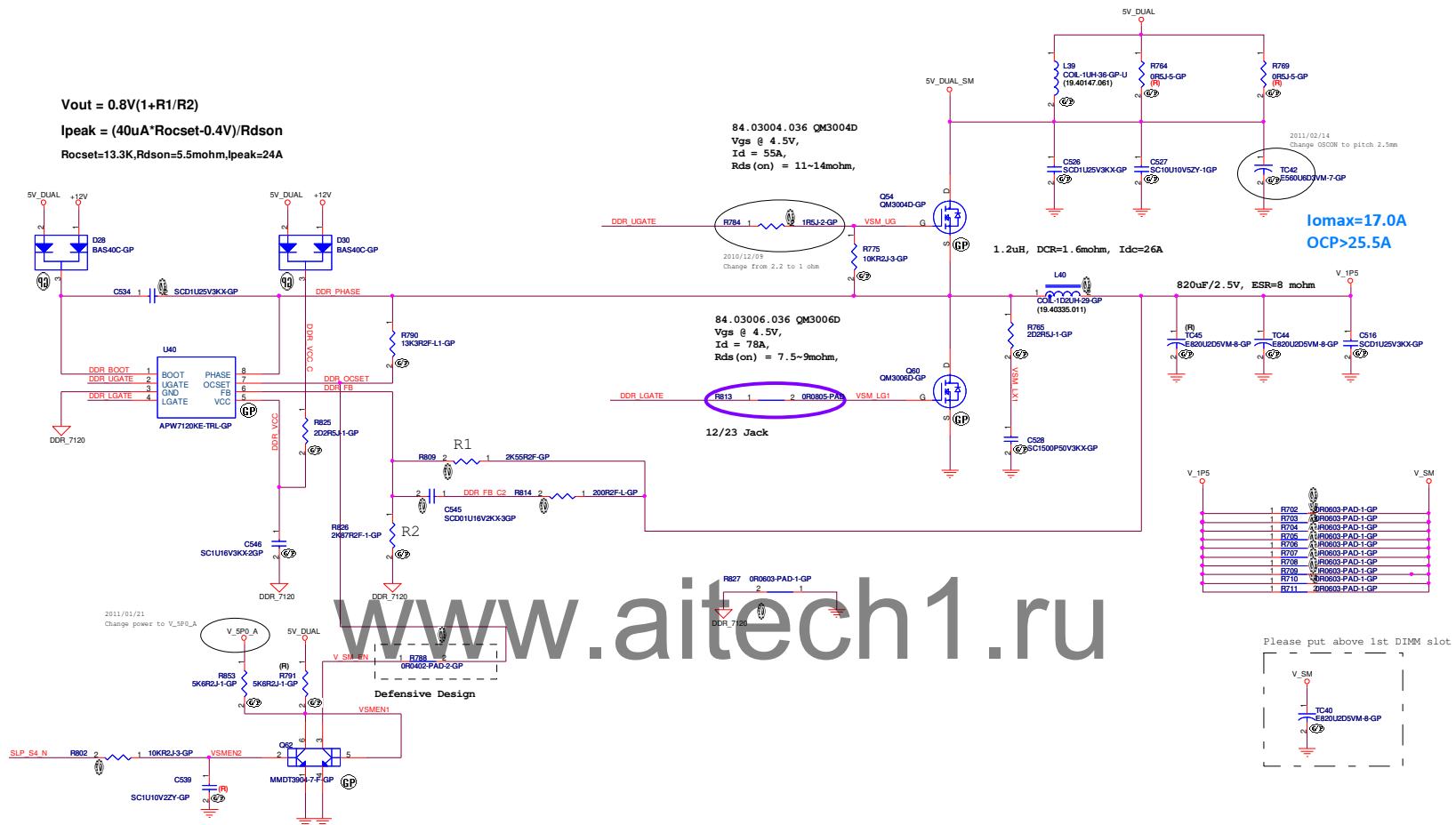
S0	S3
L	R

BACKFEED

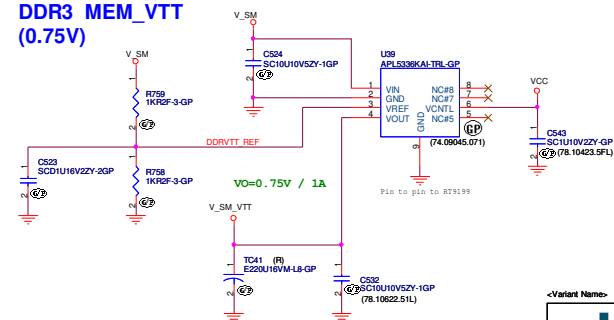
$$V_{out} = 0.8V(1+R1/R2)$$

$$I_{peak} = (40\mu A \cdot R_{ocset} - 0.4V) / R_{dson}$$

$$R_{ocset} = 13.3K, R_{dson} = 5.5m\Omega, I_{peak} = 24A$$



DDR3 MEM_VTT (0.75V)



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Wistron Incorporated
21F, 88, Hein Tai Wu Rd
Hsichih, Taipei

Title

Size

Document Number

Rev

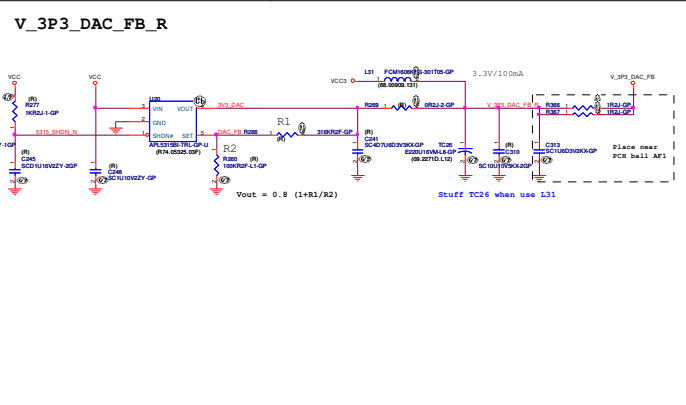
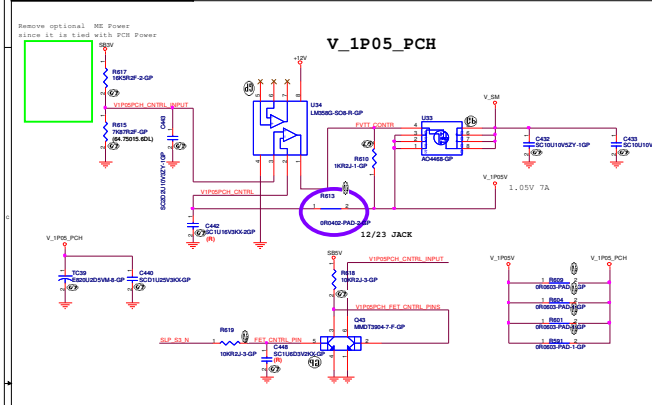
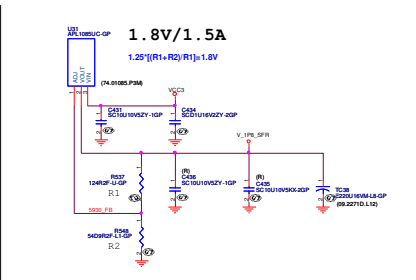
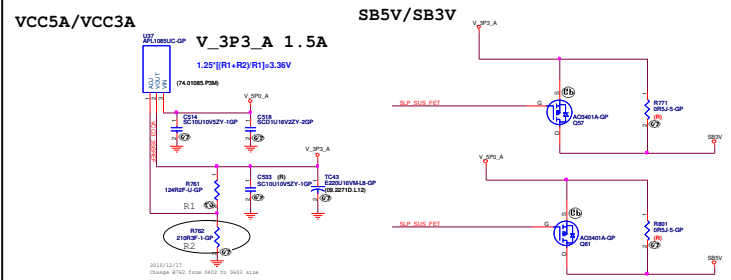
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Remove V_1P05_ME Circuit

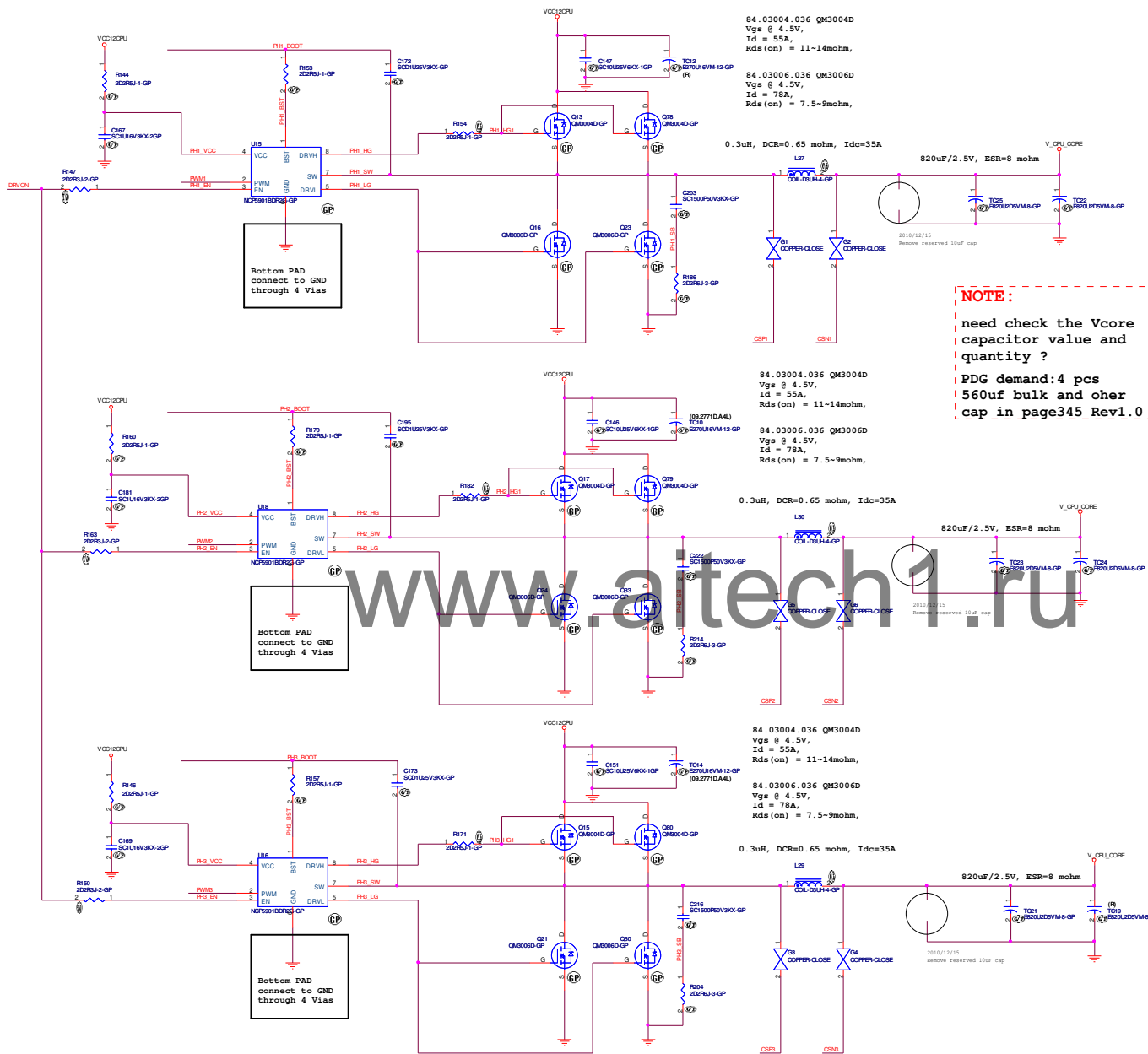
Remove ME Defensive Circuit



CPU Vcore POWER

50 DRVON >>
50 CPM1 >>
50 CPM2 >>
50 CPM3 >>
50 CPM4 >>
50 CPM5 >>
50 CPM6 >>
50 CPM7 >>
50 CPM8 >>
50 CPM9 >>
50 CPM10 >>

VCC_CORE



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